Applications Products and Business Opportunity

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Applications products and business opportunity Key messages

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The Applications business is projected to grow at ~20% CAGR with strong gross margins over the period 2020 through 2025

The Applications product portfolio supports the ASML scanner business, driven by our unique capability to help customers maximize patterning performance

- Driving improvements in Edge Placement Error (EPE)
- Delivering leading solutions for optical and e-beam metrology and inspection
- Integrating ASML's complete product portfolio into a Holistic Litho solution to optimize and control the litho process

Primary drivers of growth are the extension of our EPE roadmap:

- New metrology, inspection and control offerings extend the roadmap
- Innovative products combine computational technology, YieldStar overlay metrology and e-beam metrology
- Hardware and software products support the introduction of EUV into HVM
- New applications of deep learning in both computational litho and defect inspection drive improved performance

 Markets and product roadmap Holistic lithography
 Driving improvements in EPE
 E-beam inspection



TAM based on ASML interpretation of VLSI Research and Gartner

2020

2025

Public



Markets and product roadmap
Holistic lithography
Driving improvements in EPE
E-beam inspection

Our holistic portfolio is more important than ever



and computational metrology



Optical metrology E-beam metrology E-beam inspection ASML

Our holistic portfolio is more important than ever



Detection

ASML

Our holistic portfolio is more important than ever



Detection

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All data available at every step in the flow

Use scanner metrology, YieldStar, HMI metrology and inspection to optimize sampling for scanner control, and as yield proxy for faster time-to-yield



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Slide 10 29 Sept. 2021 Markets and product roadmap
Holistic lithography
Driving improvements in EPE
E-beam inspection

Reducing Edge Placement Error (EPE) is key to improve yield ASML Local CD errors, due to stochastics, become increasingly important

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Edge Placement Error (EPE): combined error of overlay and CD uniformity (global CDU, local CD errors and OPC error)



EPE is the best predictor of yield

YieldStar overlay metrology – after litho and after etch Characterizing the process error and enabling accurate feature placement



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Scanner actuators correct on a field-by-field basis

Tighter EPE requirements drive increased metrology ASML provides accurate, cost-effective overlay, EPE, and defect metrology

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Measurements per lot

Need for part per billion control strategy Defect-aware monitoring and control in the age of EUV stochastics

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Today, server chips can be ~800mm² in size

Need for part per billion control strategy Defect-aware monitoring and control in the age of EUV stochastics

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1 mm

1.mm

There can be >100M contact holes per mm² and increasing by 1.5x per node

Today, server chips can be ~800mm² in size

Need for part per billion control strategy Defect-aware monitoring and control in the age of EUV stochastics

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SEM image: example missing contact hole

so ~80B of these need to function

There can be >100M contact holes per mm² and increasing by 1.5x per node

Today, server chips can be ~800mm² in size Markets and product roadmap Holistic lithography Driving EPE improvements

E-beam inspection

Proc. SPIE 9778, Metrology, Inspection, and Process Control for Microlithography, 977800 (21 April 2016)

Customer design scaling Optical bright field inspection lacks sensitivity

down to 10nm feature size

Metal layer design

Optical bright field image

E-beam capable of capturing part per billion pattern fidelity defects with nanometer resolution

High resolution e-beam image

Design-based inspection

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E-beam inspection: Voltage Contrast (VC) and physical defect ASML Unique capability of electron beam inspection to find yield limiting defects

VC inspection: detection of <u>inter</u>layer defects causing electric opens and shorts

Physical inspection: detection of <u>intra</u>layer defects such as design and process weak spots

- HMI is the technology leader in e-beam inspection
- HMI leadership enabled by high current, charging control, and fast data rates

Multibeam addresses both VC and physical defect inspection ASML Delivering cost-effective throughput gains at high resolution 29 Sept. 2021

VC inspection: detection of interlayer defects causing electric opens and shorts

Physical inspection: detection of intralayer defects such as design and process weak spots

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eScan ePx

Multibeam leverages ASML core technologies ASML Increasing e-beam inspection throughput for high-volume manufacturing Slide 25 29 Sept. 2021 P(0.1 P(1,1) P(-1.0) P(0.0 P(1,0) Enhanced (Deep Learning) image Noisy (Fast Scan) image P(1,-1) Defect capture rate: 69.9% Defect capture rate: 92.8% **Throughput** 3 Brion's computational technology: Deep-learning-enabled image HMILLIN Single beam system quality enhancement **Design-based defect inspection** (2) ASML's stage technology: High speed motion **Multibeam systems** High position accuracy now shipped and installed at customers 1 HMI's Advanced Electron Optics & MEMS High quality SEM images with 9 beams scanning simultaneously

Multibeam: current status

HMIL

Implementing learnings from eScan1000 (3x3) and driving eScan1100 (5x5) qualification for first shipment expected in Q4 2021

Imaging results from the eScan1100 5x5 multibeam system

Key messages

- Multibeam technology is challenging
- We experienced some program delays: ended original development partnership, COVID
- We added additional expertise to the team and developed new multibeam IP
- We remain confident about multibeam and are committed to realizing its market potential

Status today

- 3 eScan1000 prototypes (3x3 beams) running and under assessment at customers
- System qualification of eScan1100 (5x5 beams) moving full speed; first shipment expected Q4 2021

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Forward Looking Statements

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This presentation contains statements that are forward-looking, including statements with respect to expected industry and business environment trends including expected growth, outlook and expected financial results, including expected net sales, gross margin, R&D costs, SG&A costs and effective tax rate, annual revenue opportunity for 2025, financial model for 2025 and assumptions and expected growth rates and drivers, expected growth including growth rates 2020-2025 and 2020-2030, total addressable market, growth opportunities beyond 2025 and expected annual growth rate in lithography and metrology and inspection systems and expected annual growth rate in installed base management, expected trends in addressable market up to 2030, expected trends in Logic and Memory revenue opportunities, long term growth opportunities and outlook, expected trends in demand and demand drivers, expected benefits and performance of systems and applications, semiconductor end market trends, expected growth in the semiconductor industry including expected demand growth and capital spend in coming years, expected wafer demand growth and investments in wafer capacity, expected lithography market demand and growth and spend, growth opportunities and drivers, expected trends in EUV and DUV demand, sales, outlook, roadmaps, opportunities and capacity growth and expected EUV adoption, profitability, availability, productivity and output and estimated wafer demand and improvement in value, expected trends in the applications business, expected trends in installed base management including expected revenues and target margins, expected trends and growth opportunity in the applications business, expectations with respect to high-NA, the expectation of increased output capacity. plans, strategies and strategic priorities and direction, expectation to increase capacity, output and production to meet demand, the expectation that Moore's law will continue and Moore's law evolution, product, technology and customer roadmaps, and statements and intentions with respect to capital allocation policy, dividends and share buybacks, including the intention to continue to return significant amounts of cash to shareholders through a combination of share buybacks and growing annualized dividends and statements with respect to ESG commitment, sustainability strategy, targets, initiatives and milestones. You can generally identify these statements by the use of words like "may", "will", "could", "should", "project", "believe", "anticipate", "expect", "plan", "estimate", "forecast", "potential", "intend", "continue", "target", "future", "progress", "goal" and variations of these words or comparable words. These statements are not historical facts, but rather are based on current expectations, estimates, assumptions and projections about our business and our future financial results and readers should not place undue reliance on them. Forward-looking statements do not guarantee future performance and involve a number of substantial known and unknown risks and uncertainties. These risks and uncertainties include, without limitation, economic conditions; product demand and semiconductor equipment industry capacity, worldwide demand and manufacturing capacity utilization for semiconductors, semiconductor end-market trends, the impact of general economic conditions on consumer confidence and demand for our customers' products, performance of our systems, the impact of the COVID-19 outbreak and measures taken to contain it on the global economy and financial markets, as well as on ASML and its customers and suppliers, and other factors that may impact ASML's sales and gross margin, including customer demand and ASML's ability to obtain supplies for its products, the success of R&D programs and technology advances and the pace of new product development and customer acceptance of and demand for new products, production capacity and our ability to increase capacity to meet demand, the number and timing of systems ordered, shipped and recognized in revenue, and the risk of order cancellation or push out, production capacity for our systems including the risk of delays in system production and supply chain capacity, constraints, shortages and disruptions, trends in the semi-conductor industry, our ability to enforce patents and protect intellectual property rights and the outcome of intellectual property disputes and litigation, availability of raw materials, critical manufacturing equipment and gualified employees and trends in labor markets, geopolitical factors, trade environment; import/export and national security regulations and orders and their impact on us, ability to meet sustainability targets, changes in exchange and tax rates, available liquidity and liquidity requirements, our ability to refinance our indebtedness, available cash and distributable reserves for, and other factors impacting, dividend payments and share repurchases, results of the share repurchase programs and other risks indicated in the risk factors included in ASML's Annual Report on Form 20-F for the year ended December 31, 2020 and other filings with and submissions to the US Securities and Exchange Commission. These forward-looking statements are made only as of the date of this document. We undertake no obligation to update any forward-looking statements after the date of this report or to conform such statements to actual results or revised expectations, except as required by law.

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