Role of EUV and its Business Opportunity

Hans Meiling
Vice President Product Management EUV

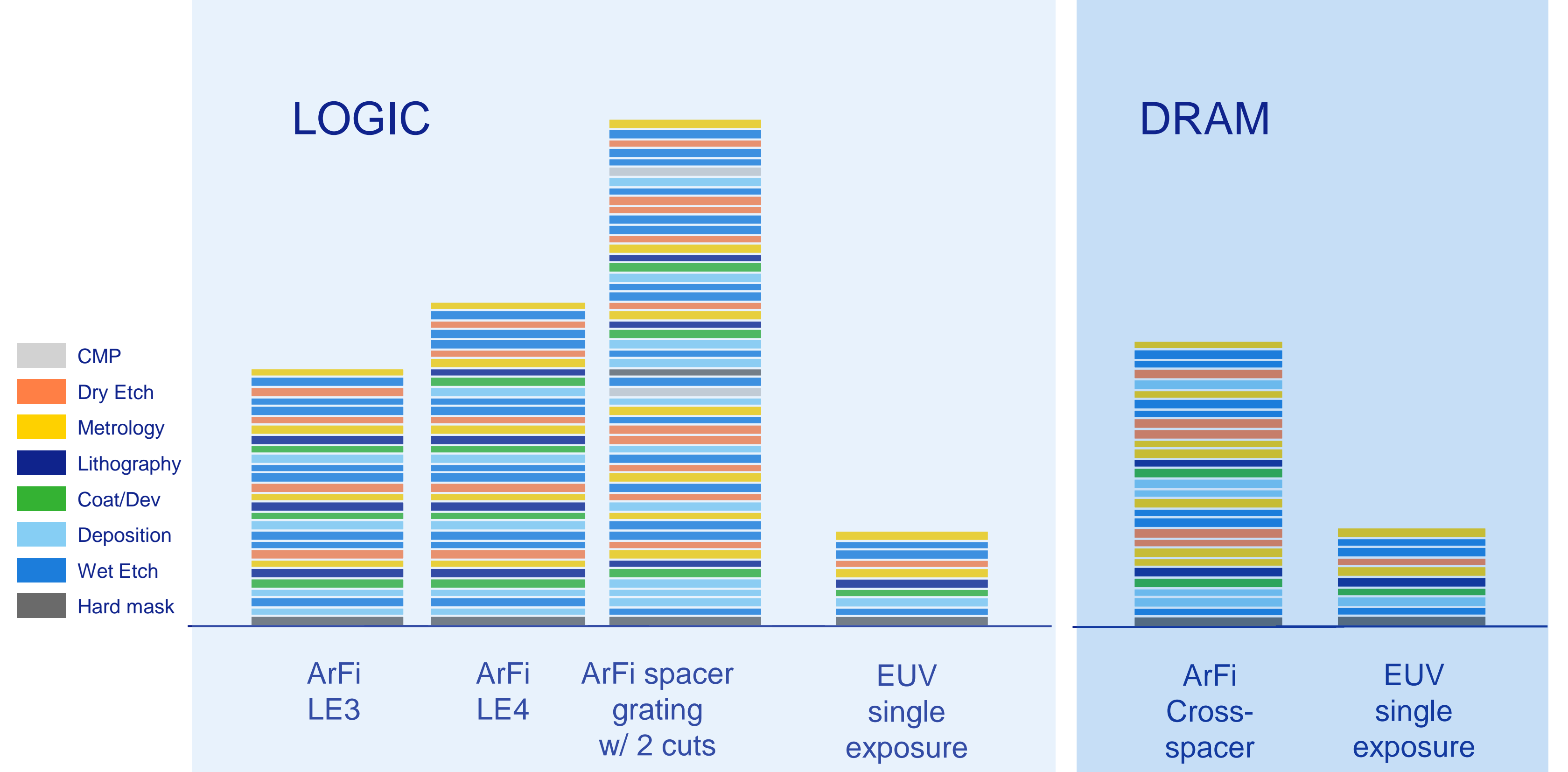
31 October 2016

Agenda

- **Why?**
- **How?**
- **When?**

EUV reduces multi-pattern process complexity

Process steps per layer



LE3=Litho+Etch+Litho+Etch+Litho+Etch

Multi-patterning complexity explodes using immersion

28 nm | 20 nm | 10 nm | 7 nm all immersion

overlay measurements

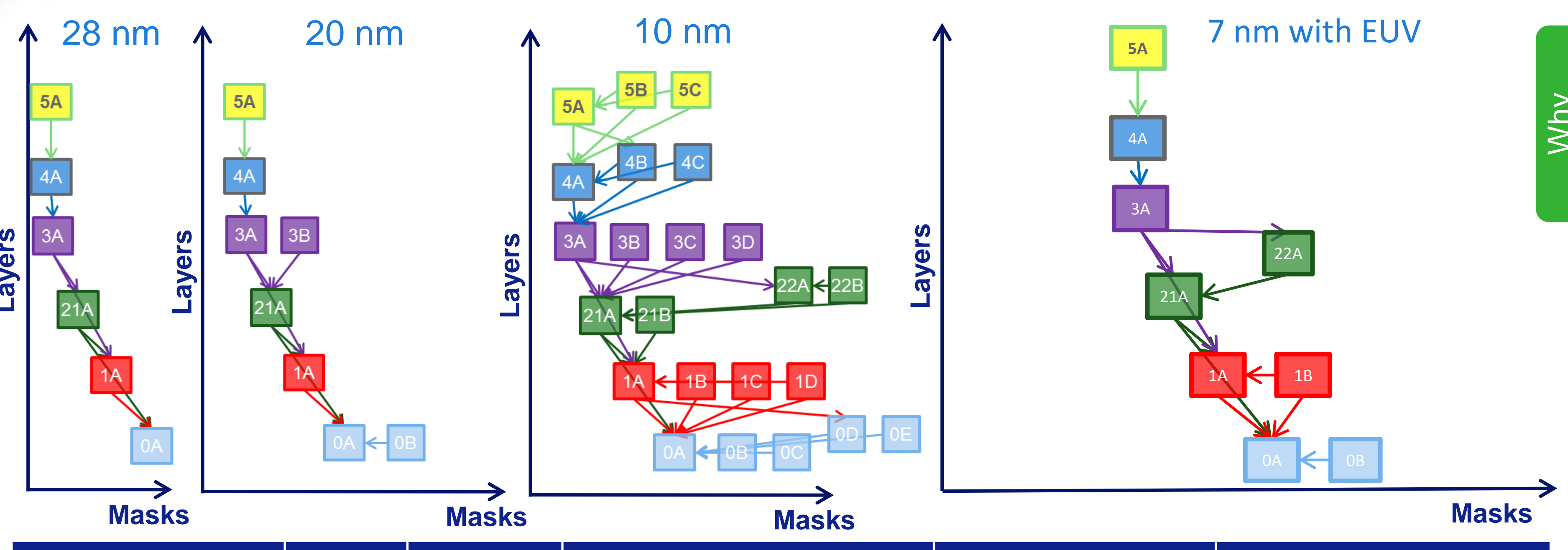
Immersion

Why

Node	28 nm
#: lithography steps	6
→: critical alignment overlay step	7

Patterning complexity reduced with EUV

through less patterning and metrology steps



Node	28 nm	20 nm	10 nm	7 nm all immersion	7 nm all EUV
#: lithography steps	6	8	23	34	9
→: critical alignment overlay step	7	9-11	36-40	59-65	12

7 nm study with leading Logic chip maker projects lower wafer cost for EUV based processes

Why

Design	Critical litho	Total Wafer Processing Cost
	54x ArF immersion	Base / FEOL / MOL / BEOL Critical / BEOL Other
	9x EUV +19x ArFi	Base / FEOL / MOL / BEOL Critical / BEOL Other (-12%)

Cost per wafer calculated for ASML cost model, all process steps

Logic motivation – lower cost, higher yield, and faster time-to-market

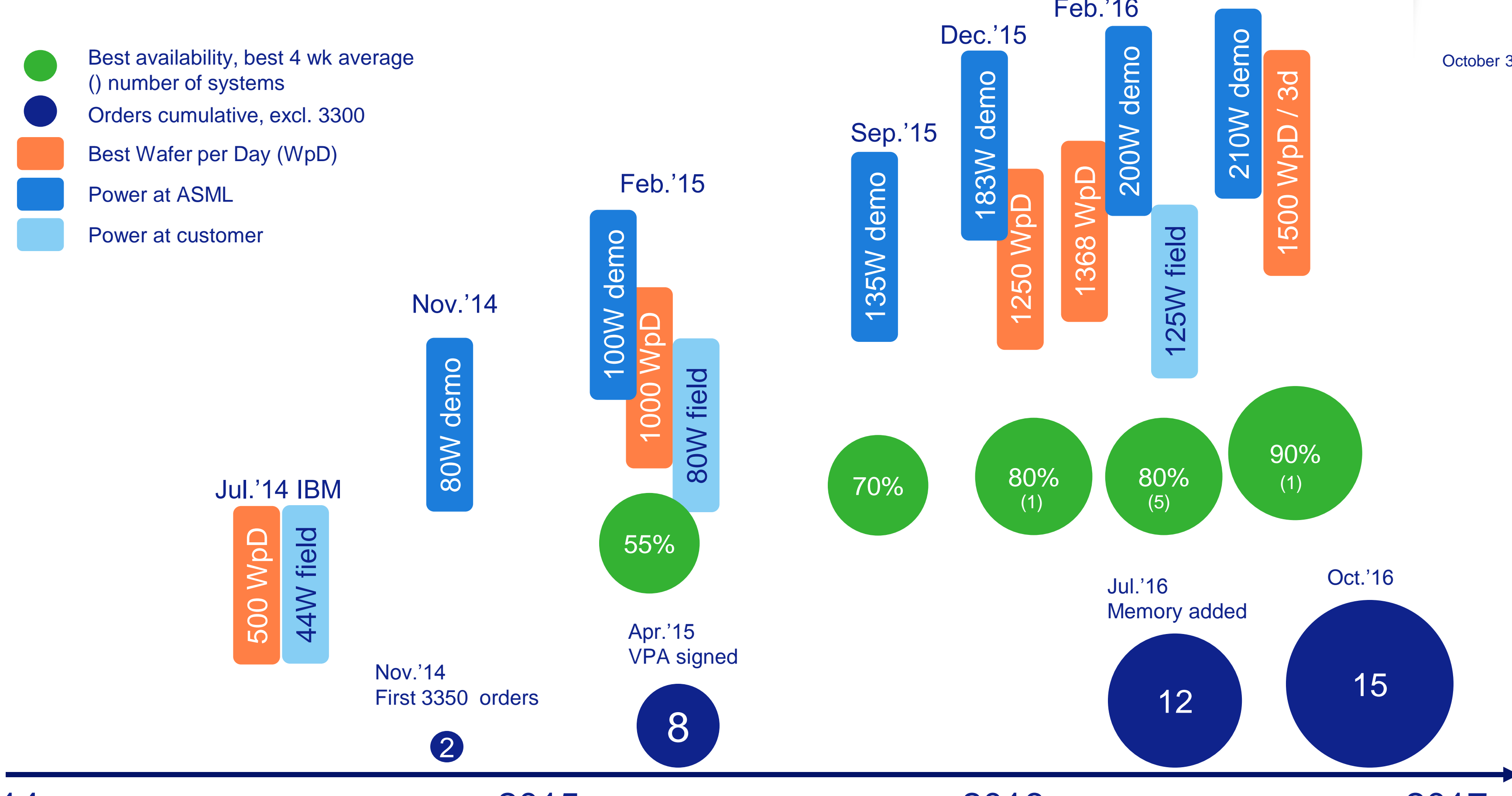
Design	Critical litho	Wafer cost	Expected Yield	Expected Time-to-Market
	54x ArF immersion	Ref.	Ref.	Ref.
	9x EUV *+19x ArFi*	-12%	+9%	-6 months

Why

Agenda

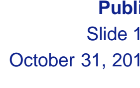
- Why?
- **How?**
- When?

EUV landscape developments



Good EUV litho performance in 14nm Pilot line

Via CD has been very stable over 1 year of operational time



How

As presented at 2016 EUVL Workshop

Intel's 14nm Pilot Line: CD trend

Resist Batch Change
Collector Swap
Resist Batch Change

Delta to Tgt (nm)
+1
0
-1
> 1 year

Delta to Tgt (nm)
+1
0
-1
> 1 year

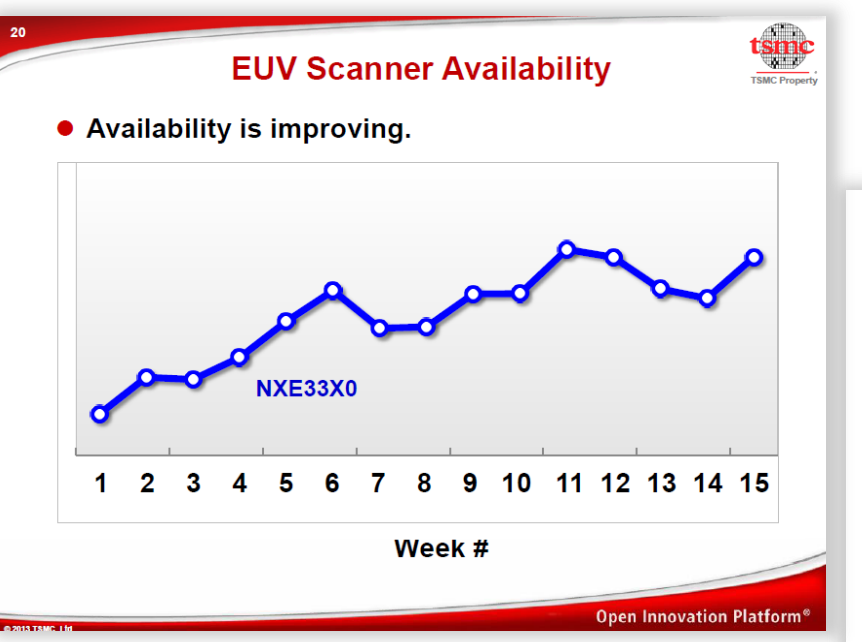
- Stable Via CD performance trend continues
- Introduction of a second tool within existing distribution

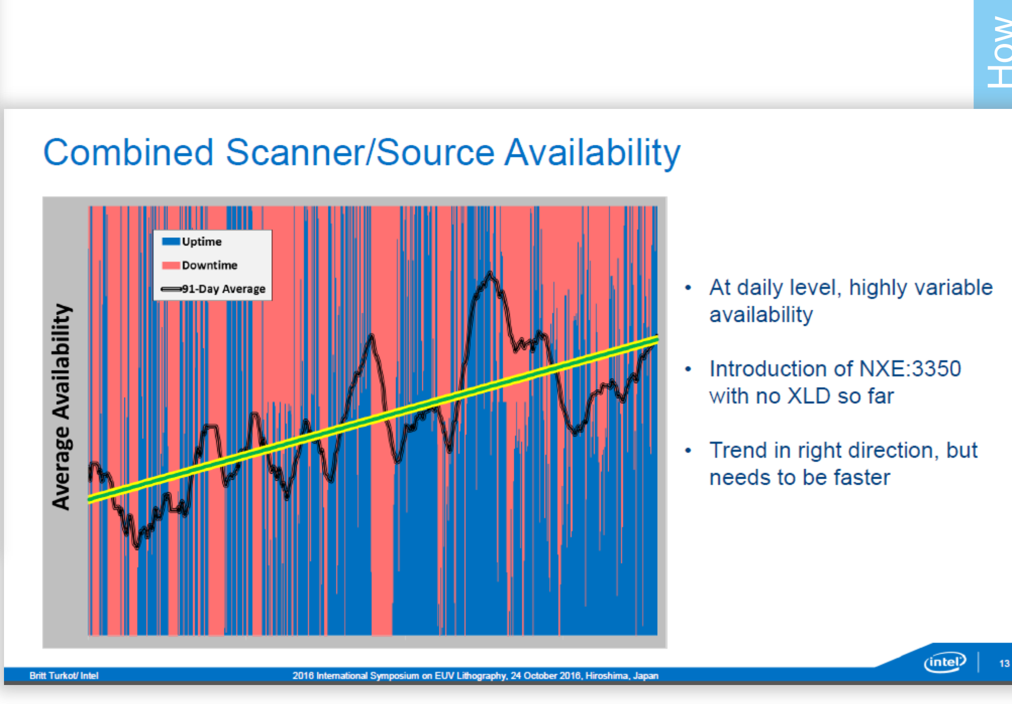
Britt Turkot/ Intel
2016 International Symposium on EUV Lithography, 24 October 2016, Hiroshima, Japan
intel

Source: Britt Turkot (Intel), EUVL Symposium, Hiroshima, Japan (24-26 Oct 2016).

Significant progress in system availability
consistency of Availability needs further improvement

How

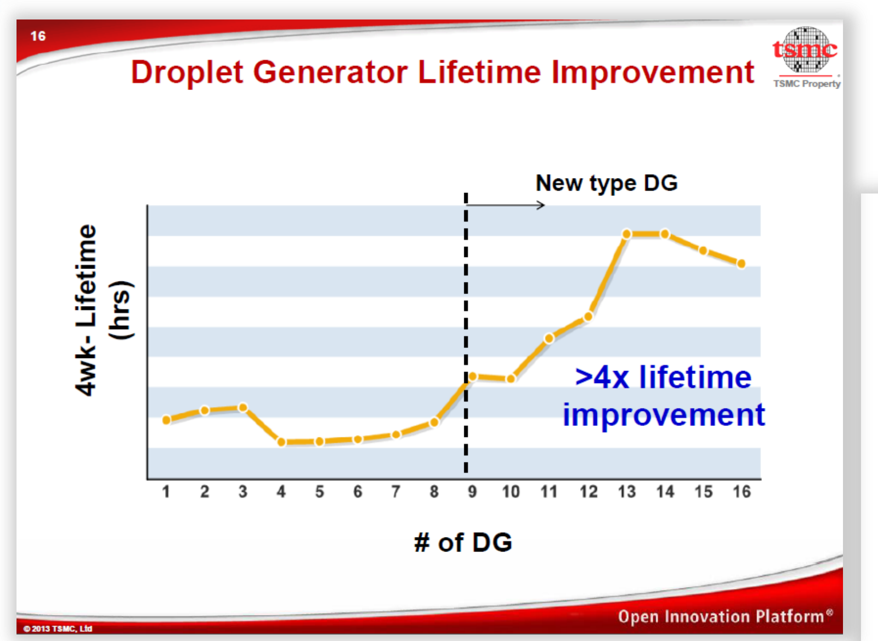




Source: Intel and TSMC presentations at EUVL Symposium, Hiroshima, Japan (24-26 Oct 2016).

Significant progress in system availability

example 1: improvements in Droplet Generator performance are recognized



As presented at 2016 EUVL Workshop

Droplet Generator: run-time and predictability improved

90%
80%
70%
30%
20%

Improved Stabilized

Improved Stabilized

Out of control

Last 1 Year

- Next step → ***increase predicted run-time***
  - Option 1: increase Sn reservoir
  - Option 2: refill Sn reservoir
- ASML developing Option 2
  - Multiple refills demonstrated
  - Refill G2G << swap G2G

- >3X increase in run-time
- Improved predictability in actual vs. expected run-time

Britt Turkot/ Intel
2016 International Symposium on EUV Lithography, 24 October 2016, Hiroshima, Japan
intel
8

How

Source: Intel and TSMC presentations at EUVL Symposium, Hiroshima, Japan (24-26 Oct 2016).

Roadmap in place towards >90% availability

Significant progress since 2014, consistency must be improved

How

System Availability [%]
Max. 4 weeks average

100
90
80
70
60
50
40
30
20
10
0

2014 | 2015 | 2016 | 2017 target | 2018 target

Time

2015

Collector lifetime:
- Flows, heated vanes

Droplet Generator:
- Warm swap tool

Seed Table:
- EOM, seed laser reliability

2016

Droplet Generator:
- Tin refill

Collector swap time

Tin catch:
- In-line draining

2017 target

Droplet Generator:
- In-line tin refill

Seed Table:
- High Power Seed Table

Drive Laser
- MTBI / MTTR improvements

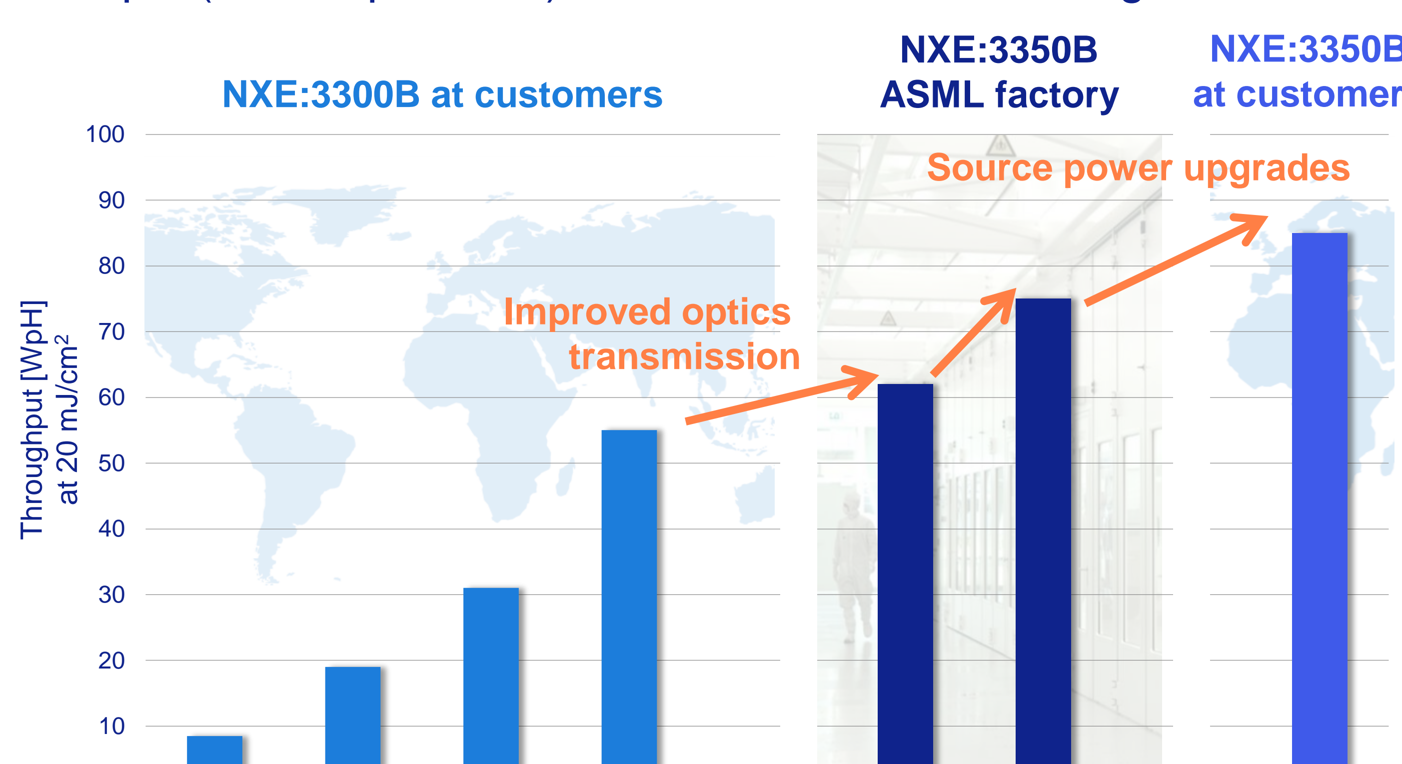
2018 target

Droplet Generator:
- Continuous refill

Scanner and source
- MTBI / MTTR improvements
- Improved diagnostics

Productivity continues to improve

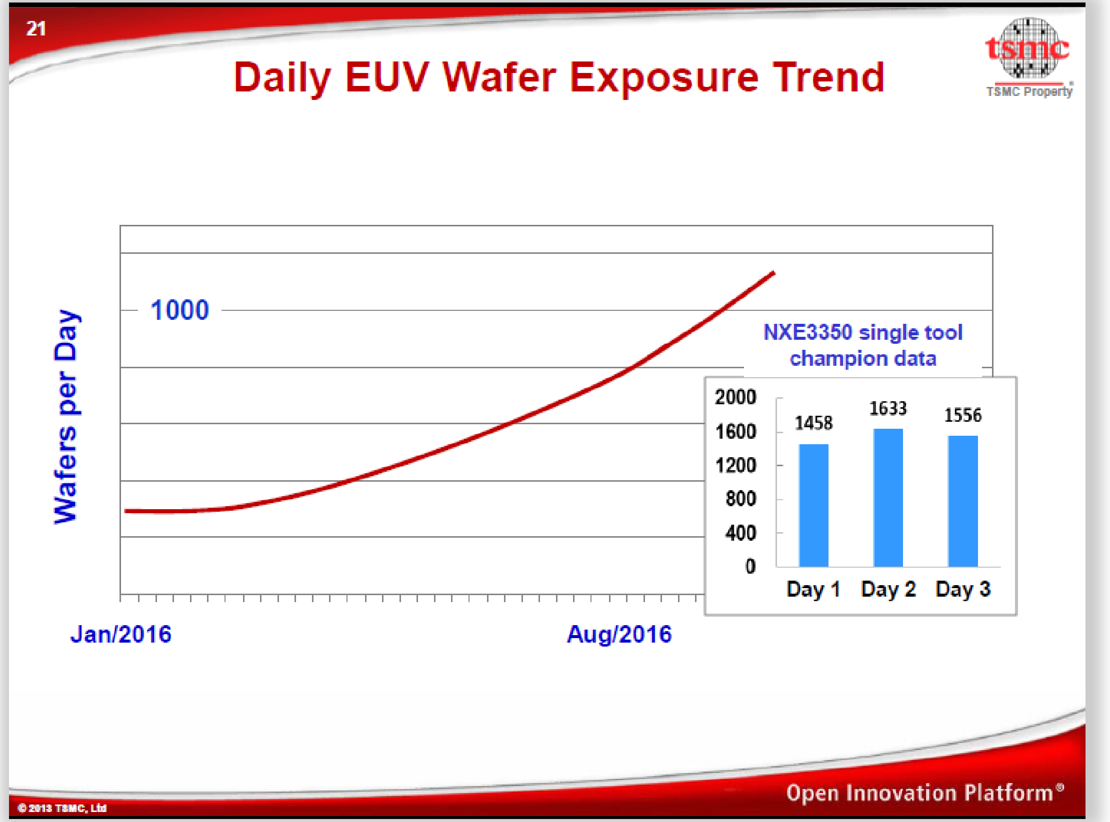
85 WpH (wafers per hour) achieved with 125W configuration



NXE:3350B ATP test: 26x33mm2, 96 fields, 20mJ/cm^2

Productivity improvement also available to customers

3-day average of >1500 WpD achieved on NXE:3350B

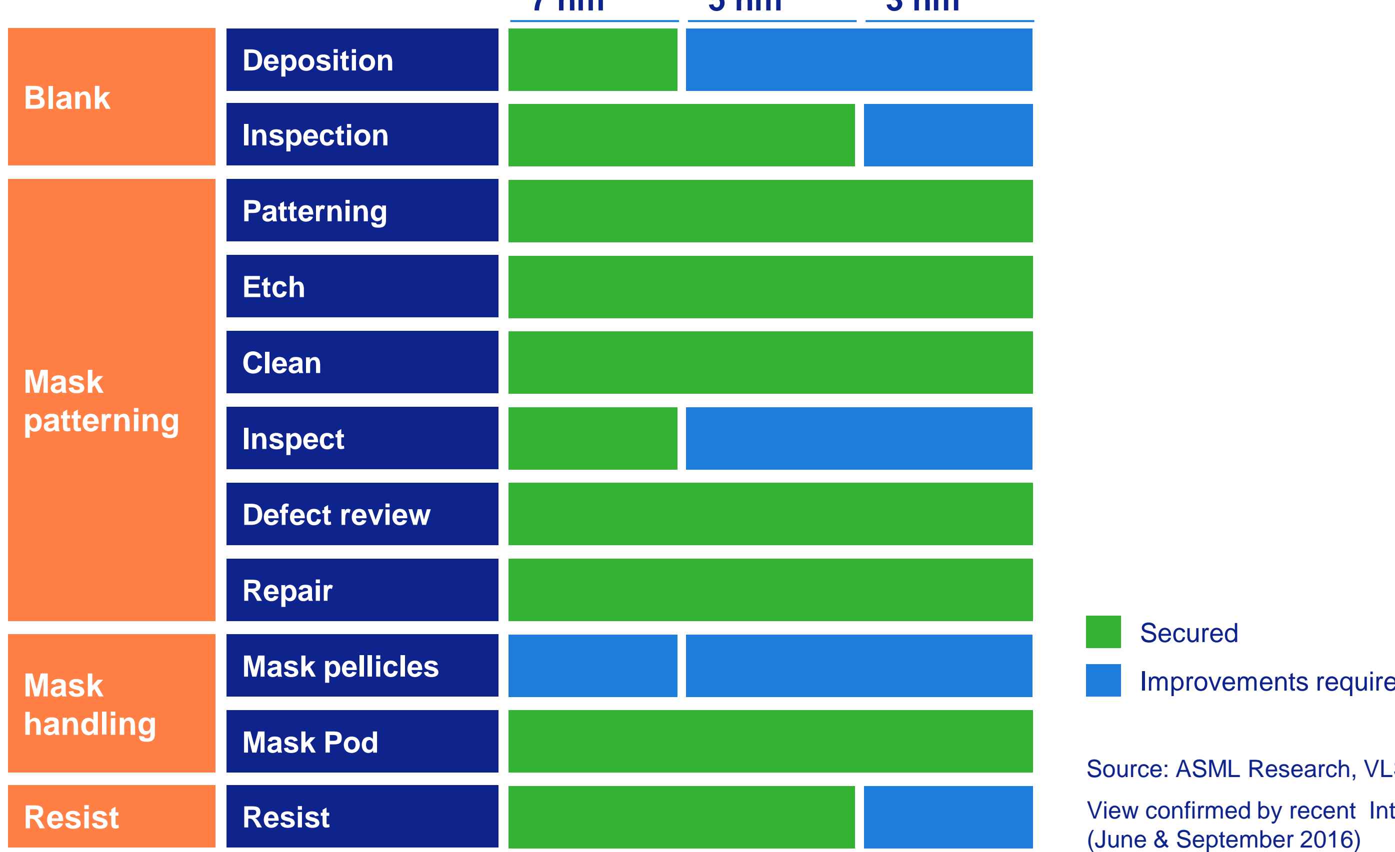


Source: L.J. Chen (TSMC), EUVL Symposium, Hiroshima, Japan (24-26 Oct 2016).

Throughput roadmap towards >125 WpH in place

EUV infrastructure is viable for 7 nm node

improvements required for 5 nm



Secured

Improvements required

Source: ASML Research, VLSI

View confirmed by recent Intel reports (June & September 2016)

Evolution of Infrastructure readiness

How

From 2014 Source Workshop

EUV Infrastructure Readiness Snapshot

EUV infrastructure ha
1 is ready now, 4 are in de

- E-beam Mask Insp
- AIMS Mask Inspect
- Actinic Blank Inspe
- Pellicle: C&F result
- EUV blank quality:
- Actinic Patterned M Industry developme
- Blank multi-layer d techniques being ev
- EUV resist QC: Rap

From 2015 EUVL Workshop

EUV Infrastructure Readiness Snapshot

EUV infrastructure has 8 key programs
2 are ready or near-ready now

- E-beam Mask Inspectio
- Actinic Blank Inspectio
- EUV resist QC: Industry
- AIMS Mask Inspection:
- EUV blank quality: Pro
- Pellicle: ASML commer
- Blank multi-layer depo techniques being evalua
- Post-pellicle mask insp options.

Mark Phillips / Intel

From 2015 EUV Source Workshop

EUV Infrastructure Readiness Snapshot

EUV infrastructure has 8 key programs
2 are ready or near-ready now, 5 are in development, 1 has significant gaps

- E-beam Mask Inspe
- AIMS Mask Inspect
- Actinic Blank Inspe
- Pellicle: ASML com
- EUV blank quality:
- Actinic Patterned M actinic inspection in
- Blank multi-layer d techniques being ev
- EUV resist QC: QC

Britt Turkot / Intel 2015 International

Judged as of Today

EUV Infrastructure Readiness Snapshot

EUV infrastructure has 8 key programs
3 are ready or near-ready now, 4 are in development, 1 has significant gaps

- **E-beam Mask Inspection**: In use for low volume production. Need TPT increase.
- **Actinic Blank Inspection (ABI)**: Ready for qualification of HVM quality blanks
- **AIMS Mask Inspection**: Imaging demonstrated; systems shipping to field
- **Pellicle**: ASML commercializing – needs acceleration; production phase in 2H'17 – cannot slip schedule
- **EUV blank quality**: Process and yield improvements continue
- **Blank multi-layer deposition tool**: Improving defect results. Multiple deposition techniques being evaluated to define HVM tool approach.
- **EUV resist QC**: RMQC center at IMEC expected online in 2017
- **Actinic Patterned Mask Inspection (APMI)**: High resolution PWI for fab. Still need actinic inspection in mask shop.

Britt Turkot/ Intel 2016 International Symposium on EUV Lithography, 24 October 2016, Hiroshima, Japan

Source: Britt Turkot (Intel), EUVL Symposium, Hiroshima, Japan (24-26 Oct 2016).

Continued improvement in mask defects will lead to yield improvements

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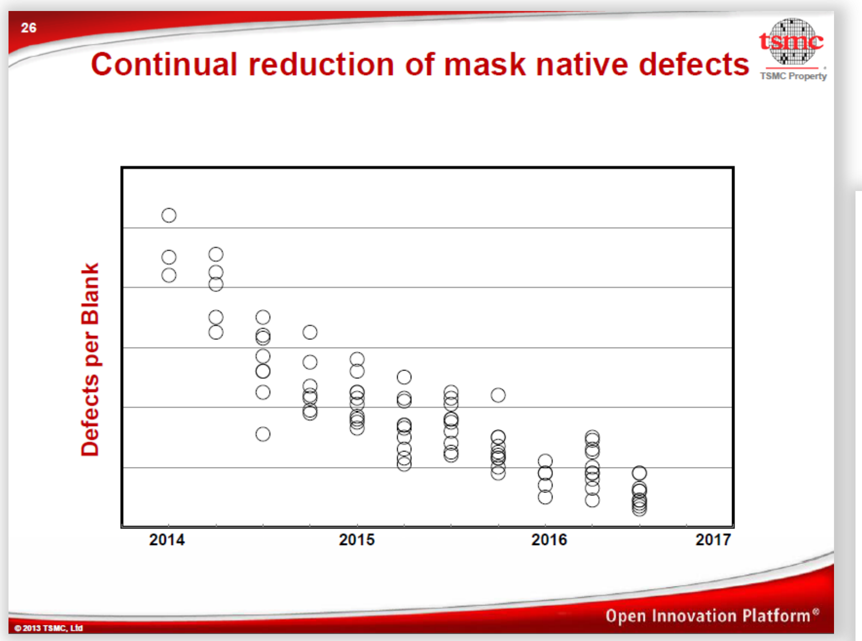
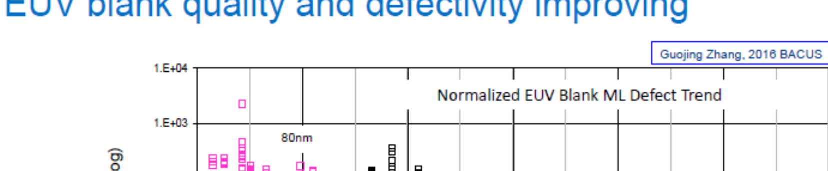
How



From 2016 BACUS

EUV blank quality and defectivity improving



- Progress continues in blank ML defect reduction; continued yield improvement is expected.
- Higher sensitivity blank inspection with better defect location accuracy needs to be integrated in the blank manufacturing process.
- Substrate flatness and reflectivity trending to target.

Britt Turkot/ Intel 2016 International Symposium on EUV Lithography, 24 October 2016, Hiroshima, Japan intel 26

Source: Intel and TSMC presentations at EUVL Symposium, Hiroshima, Japan (24-26 Oct 2016).

NXE Pellicles are being mounted and used in scanners

Durability measured to >85 WpH

Pellicle on integration mounting tooling

Progress resist materials: towards 16 nm resolution
at 125 WpH

	16 nm Horizontal Dense lines/spaces			13 nm Horizontal Dense lines/spaces	
	NXE:3350 Reference CAR	New formulation CAR	New Inpria resist (NTI non-CAR)	CAR	Non-CAR
SEM image @BE/BF (90deg rotated)					
Dose	40 mJ/cm²	25 mJ/cm²	**18.5 mJ/cm²**	~40 mJ/cm²	31 mJ/cm²
LWR	4.6 nm	5.2 nm	4.4 nm	4.5 nm	4.2 nm

Productivity improvement

Imaging improvement

Inpria

How

Exposures done on NXE:3350B system with Dipole Y illumination. LWR: Line Width Roughness

Inpria

Agenda

- Why?
- How?
- **When?**

Public

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Industry Shrink Roadmap & EUV insertion

EUV Production Insertion Window

HVM	2014	2015	2016	2017	2018	2019	2020	2021	2022

Logic

20nm → 16/14nm → 10nm → 7nm → 5nm → 3nm

Node name

Performance Memory

DRAM

28-30 → 20-22 → 1X → 1Y → 1Z → next

Minimum half pitch

Storage Class Memory

PC-RAM, ReRAM, X-point etc.

2X'/x2 → 1X"/x4 → 1Y"/x8 → 1Z"/x8

Minimum half pitch /x number of layers

Storage Memory

Planar Floating Gate NAND

22 → 17-18 → 14-15

3D NAND

x24 → x32 → x48 → x64 → >x96 → >x128 → >x192 → >x200

x number of layers

☆ Customer comments on EUV insertion (see next slide)

When

Today's status

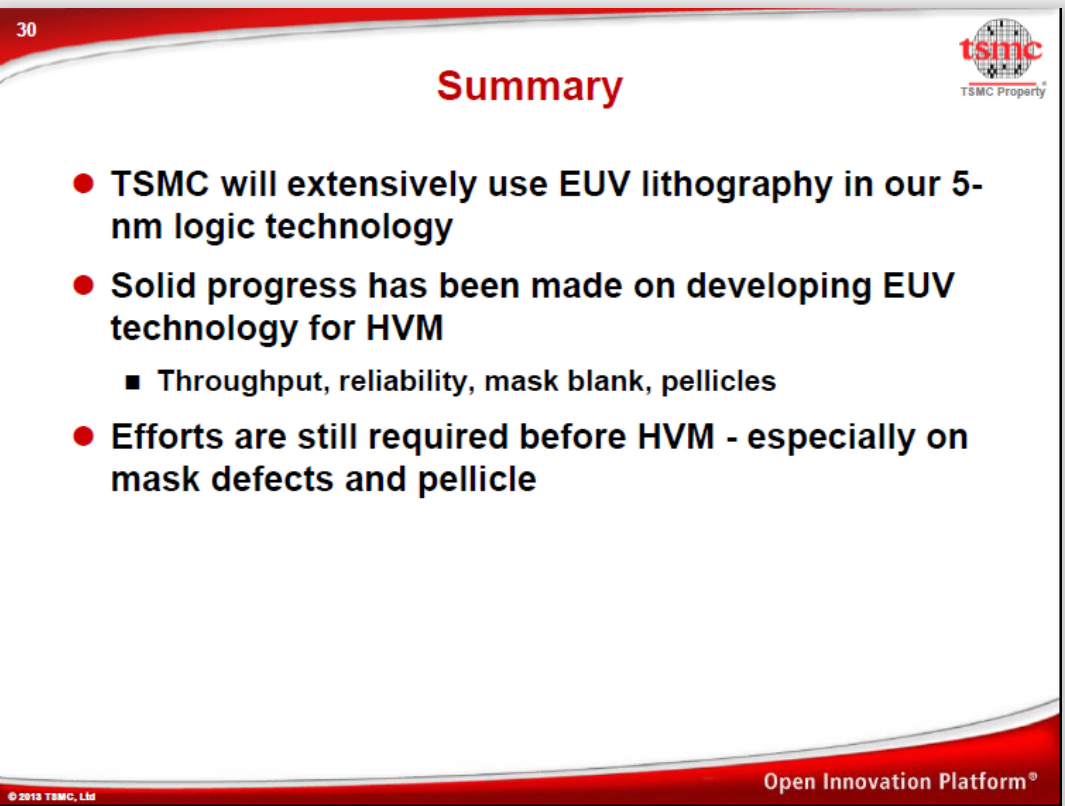
- Production[1]
- Development[1]
- Research[1]
- Roadmap[2]

Source: 1) Customers - public statements,, IC Knowledge LLC; 2) ASML extrapolations

Customers plan to insert EUV into production in 2018/19

When

Customer public statements on EUV HVM insertion



Source: L.J. Chen (TSMC), EUVL Symposium, Hiroshima, Japan (24-26 Oct 2016).

Customers plan to insert EUV into production in 2018/19

When

Customer public statements on EUV HVM insertion

Mark Liu - President & Co-CEO, Q3 2016 Earnings Call

- *Since the beginning of this year, our 5nm technology has graduated from pathfinding to enter technology development phase.*
- *Recently, our EUV technology development made good progress.*
- *The throughput and the reliability of the EUV scanner, the sensitivity of EUV photoresist and the quality of EUV mask blank and pellicles all improved.*
- *Of course, there's still a way to go.*
- *We will use EUV lithography extensively in our 5nm flow to improve density, simplify process steps and reduce cost.*
- *A plan of risk production qualification in first half of 2019 remains unchanged.*

Mark Bohr, IDF, august 2016

- *ArFi is the primary flow for 7nm and EUV will be inserted when it is ready.*
- *Improvements are still needed in uptime/availability and throughput.*
- *EUV could replace ArFi layers in the 7nm flow once ready.*

Sanjay Jha-CEO, Sep 2016, Globalfoundries Technology Conference regarding 7 nm

- *the new process will include the equipment for Extreme Ultraviolet (EUV) lithography,*
- *.. will not be reliant solely on EUV and will have the option of using an optical process at 7 nm if EUV proves to still be impractical.*
- *Without EUV, however, the 7nm node is anticipated to require upwards of 84 mask steps.*

Seong-Sue Kim- SPIE Conference Feb 2016

"… Both the source power and the availability progress are on track and with current trend EUV is expected to be used for 7nm production"

Source: Customer public statements

Customers plan to insert EUV into production in 2018/19

When

Customer public statements on EUV HVM insertion

Kim Jun-Ho, Q2 2016 Earnings call:
"…we also are planning to start the development for the 1Y nano and for this, EUV that has been used for R&D, … whether EUV will be adopted in full for 1Y nano, we cannot say at this point. But one thing is for sure and that is we will use EUV for mass production of 1Z nano and that is going to be in 2019."

Seong-Sue Kim- SPIE Conference Feb 2016
… Feasibility proved for both L7 and D1Y patterning "

Source: Customer public statements

EUV extension roadmap

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introduction	55 WPH	125 WPH	145 WPH	185 WPH	Overlay [nm]
2013	NXE:3[illegible]B				7
2015		[illegible]350B			3.5
2017		NXE:3400B			3
			NXE:next		<3
				High [illegible]	<2

At customer upgradable

New platform

products under study

Roadmap: October 2016

EUV estimated demand per fab by market

Range of layers and corresponding systems per fab*

When

Market	Fab Capacity (kwspm)	EUV layers	EUV systems/fab	ArFi systems/fab
Logic	45	6 - 10	7 - 12	21 - 16
Performance Memory	100	1 - 2	2 - 4	16 - 14
Storage Class Memory (ie. ReRAM)	80	0 or 9	0 or 13	18 or 6

kwspm: x1000 wafer starts per month

*"Typical" process and system conditions in the 2018-2020 timeframe, not specific customer condition

EUV facilities and supply chain supports demand

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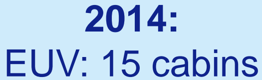
When

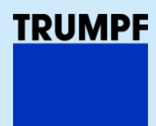


2014:
EUV: 15 cabins

2015:
new EUV cleanroom: +10 cabins

201x:
EUV: +10 cabins when needed, shell ready

EUV factory cleanrooms in place



New cleanroom announced in June 2015

EUV summary

Availability

- Best performance is four-week average above 90% on a NXE:3300B system
- Seven customer systems have achieved a four-week average availability >80%, consistency between tools and across sites still needs to be significantly improved
- Roadmap to >90% availability, with consistent performance, in place

Productivity

- More than 1,500 wafers per day (WpD) exposed on a NXE:3350B at a customer site on average over three days at 85WpH configuration. Roadmap in place to secure >125WpH

Infrastructure

- EUV infrastructure is developing in sync with 7nm node insertion timing; further improvements required for 5nm node

Insertion

- ASML expects that customers will take EUV into production in 2018-2019 timeframe

Forward looking statements

This document contains statements relating to certain projections and business trends that are forward-looking, including statements with respect to our outlook, including expected customer demand in specified market segments (and underlying assumptions) including memory, logic and foundry, expected sales levels, trends, including trends towards 2020 and beyond and expected industry growth, and outlook, systems backlog, expected or indicative market opportunity, financial results and targets, including, for ASML and ASML and HMI combined, expected sales, other income, gross margin, R&D and SG&A expenses, capital expenditures, cash conversion cycle, EPS and effective annualized tax rate, annual revenue opportunity and EPS potential by end of decade and growth opportunity beyond 2020 for ASML and ASML and HMI combined, cost per function reduction and ASML system ASP, goals relating to gross cash balance and ASML's capital structure, customer, partner and industry roadmaps, productivity of our tools and systems performance, including EUV system performance (such as endurance tests), expected industry trends and expected trends in the business environment, the addition of value through delivery of lithography products and the achievement of cost-effective shrink, expected continued lithography demand and increasing lithography spend, the main drivers of lithography systems, lithography intensity for all market segments, customer execution of shrink roadmaps, future memory application distribution, expected addressable markets, including the market for lithography systems and service and options, expected manufacturing and process R&D, statements with respect to growing end markets that require fab capacity driving demand for ASML's tools, statements with respect to the acquisition of HMI by ASML, including market opportunity, the expected timing of completion of the HMI acquisition and delisting of HMI, the expected benefits of the acquisition of HMI by ASML, including expected continuation of year on year growth, the provision of e-beam metrology capability and its effect on holistic lithography solutions, including the introduction of a new class of pattern fidelity control and the improvement of customers' control strategy, statements with respect to EUV, including targets, such as availability, productivity, facilities and shipments, including the number of EUV systems expected to be shipped and timing of shipments, and roadmaps, shrink being key driver to industry growth, expected industry adoption of EUV and statements with respect to plans of customers to insert EUV into production and timing, the benefits of EUV, including expected cost reduction and cost-effective shrink, the expected continuation of Moore's law, without slowing down, and that EUV will continue to enable Moore's law and drive long term value, goals for holistic lithography, including pattern fidelity control, expectations relating to double patterning, immersion and dry systems, intention to return excess cash to shareholders, statements about our proposed dividend, dividend policy and intention to repurchase shares and statements with respect to the current share repurchase plan. You can generally identify these statements by the use of words like "may", "will", "could", "should", "project", "believe", "anticipate", "expect", "plan", "estimate", "forecast", "potential", "intend", "continue" and variations of these words or comparable words. These statements are not historical facts, but rather are based on current expectations, estimates, assumptions and projections about the business and our future financial results and readers should not place undue reliance on them.

Forward-looking statements do not guarantee future performance and involve risks and uncertainties. These risks and uncertainties include, without limitation, economic conditions, product demand and semiconductor equipment industry capacity, worldwide demand and manufacturing capacity utilization for semiconductors (the principal product of our customer base), including the impact of general economic conditions on consumer confidence and demand for our customers' products, competitive products and pricing, the impact of any manufacturing efficiencies and capacity constraints, performance of our systems, the continuing success of technology advances and the related pace of new product development and customer acceptance of new products including EUV, the number and timing of EUV systems expected to be shipped and recognized in revenue, delays in EUV systems production and development, our ability to enforce patents and protect intellectual property rights, the risk of intellectual property litigation, availability of raw materials and critical manufacturing equipment, trade environment, changes in exchange rates, changes in tax rates, available cash and liquidity, our ability to refinance our indebtedness, distributable reserves for dividend payments and share repurchases and timing of resumption of the share repurchase plan, and other risks indicated in the risk factors included in ASML's Annual Report on Form 20-F and other filings with the US Securities and Exchange Commission. These forward-looking statements are made only as of the date of this document. We do not undertake to update or revise the forward-looking statements, whether as a result of new information, future events or otherwise.

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