Public

BAML 2019 APAC TMT Conference

EUV: Enabling cost efficiency, tech innovation and future industry growth

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Taipei, Taiwan
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Forward Looking Statements

This document contains statements relating to certain projections, business trends and other matters that are forward-looking, including statements with respect to expected trends and outlook, strategy, bookings, expected financial results and trends, including expected sales, EUV revenue, gross margin, capital expenditures, R&D and SG&A expenses, cash conversion cycle, and target effective annualized tax rate, and expected financial results and trends for the rest of 2018 and 2019, expected revenue growth and demand for ASML's products in logic and memory, expected annual revenue opportunity in 2020 and for 2025 and expected EPS potential in 2020 with significant growth in 2025, expected trends in the lithography system market, fab capacity by segment, the automotive and artificial intelligence industries, connectivity, semiconductor end markets and new semiconductor nodes, expected acceleration of chipmakers' performance for the next decade, expected EUV insertion and transistor density growth, trends in DUV systems revenue and Holistic Lithography and installed based management revenues, statements with respect to expectations regarding future DUV sales, including composition, margins, improvement of operations and performance, DUV product roadmaps, expected benefits of the holistic productivity approach, including in terms of wafers per year, expected industry trends and expected trends in the business environment, statements with respect to customer demand and the commitment of customers to High NA machines and to insert EUV into volume manufacturing by ordering systems, expected future operation of the High NA joint lab, statements with respect to holistic lithography roadmaps and roadmap acceleration, including the introduction of higher productivity systems in 2019 (including the expected shipment of NXE:3400C and expected timing thereof) and the expected benefits, ASML's commitment to volume manufacturing and related expected plans until 2030, ASML's commitment to secure system performance, shipments, and support for volume manufacturing, including availability, timing of and progress supporting EUV ramp and improving consistency, productivity, throughput, and production and service capability enabling required volume as planned, including expected shipments, statements with respect to growth of fab capacity driving demand in lithography systems, planned customer fabs for 200 systems and expected first output in 2019, expected EUV value increase and increase in EUV margins and ASML's expectation of EUV profitability at the DUV level, expected installed base of EUV systems, expected customer buildout of capacity for EUV systems, EUV estimated demand by market, expected increase in lithography intensity, statements with respect to the expected benefits of EUV, including year-on-year cost reduction and system performance, and of the introduction of the new DUV system and expected demand for such system, the expected benefits of HMI's e-beam metrology capabilities, including the expansion of ASML's integrated Holistic Lithography solutions through the introduction of a new class of pattern fidelity control, the extension of EUV to enable cost effective single patterning shrink with EUV, statements with respect to ASML's applications business, including statements with respect to expected results in 2018, expected growth of the applications business and expected drivers of growth, expected growth in margins, continued shrink and drivers, and expected accuracy, defect control and performance improvements, shrink being a key driver supporting innovation and providing long-term industry growth, lithography enabling affordable shrink and delivering value to customers, DUV, Holistic Lithography and EUV providing unique value drivers for ASML and its customers, expected industry innovation, the expected continuation of Moore's law and that EUV will continue to enable Moore's law and drive long term value for ASML beyond the next decade, intention to return excess cash to shareholders through stable or growing dividends and regularly timed share buybacks in line with ASML's policy, statements with respect to the expectation to continue to return cash to shareholders through dividends and share buybacks, and statements with respect to the expected impact of accounting standards. You can generally identify these statements by the use of words like "may", "will", "could", "should", "project", "believe", "anticipate", "expect", "plan", "estimate", "forecast", "potential", "intend", "continue", "targets", "commits to secure" and variations of these words or comparable words. These statements are not historical facts, but rather are based on current expectations, estimates, assumptions and projections about the business and our future financial results and readers should not place undue reliance on them.

Forward-looking statements do not guarantee future performance and involve risks and uncertainties. These risks and uncertainties include, without limitation, economic conditions, product demand and semiconductor equipment industry capacity, worldwide demand and manufacturing capacity utilization for semiconductors, including the impact of general economic conditions on consumer confidence and demand for our customers' products, competitive products and pricing, the impact of any manufacturing efficiencies and capacity constraints, performance of our systems, the continuing success of technology advances and the related pace of new product development and customer acceptance of and demand for new products including EUV and DUV, the number and timing of EUV and DUV systems shipped and recognized in revenue, timing of EUV orders and the risk of order cancellation or push out, EUV production capacity, delays in EUV systems production and development and volume production by customers, including meeting development requirements for volume production, demand for EUV systems being sufficient to result in utilization of EUV facilities in which ASML has made significant investments, potential inability to successfully integrate acquired businesses to create value for our customers, our ability to enforce patents and protect intellectual property rights, the outcome of intellectual property litigation, availability of raw materials, critical manufacturing equipment and qualified employees, trade environment, changes in exchange rates, changes in tax rates, available cash and liquidity, our ability to refinance our indebtedness, distributable reserves for dividend payments and share repurchases, results of the share repurchase plan and other risks indicated in the risk factors included in ASML's Annual Report on Form 20-F and other filings with the US Securities and Exchange Commission. These forward-looking statements are made only as of the date of this document. We do not undertake to update or revise the forward-looking statements, whether as a result of new information, future events or otherwise.

Agenda

- Today's Advanced Lithography Technology
- Tech innovation and future growth drivers
  - 5G connectivity, Artificial Intelligence, Autonomous Driving, Big Data, Emerging Memory
- Lithography's role in semiconductor manufacturing now and in the future

And this happens 50,000 times every second, of every minute, of every hour, of every day…month…year….

Backlight shadowgram from a NXE:3300 EUV source

As a frame of reference…..What else happens in a second?

A spark plug ignites
16.67 sparks per second

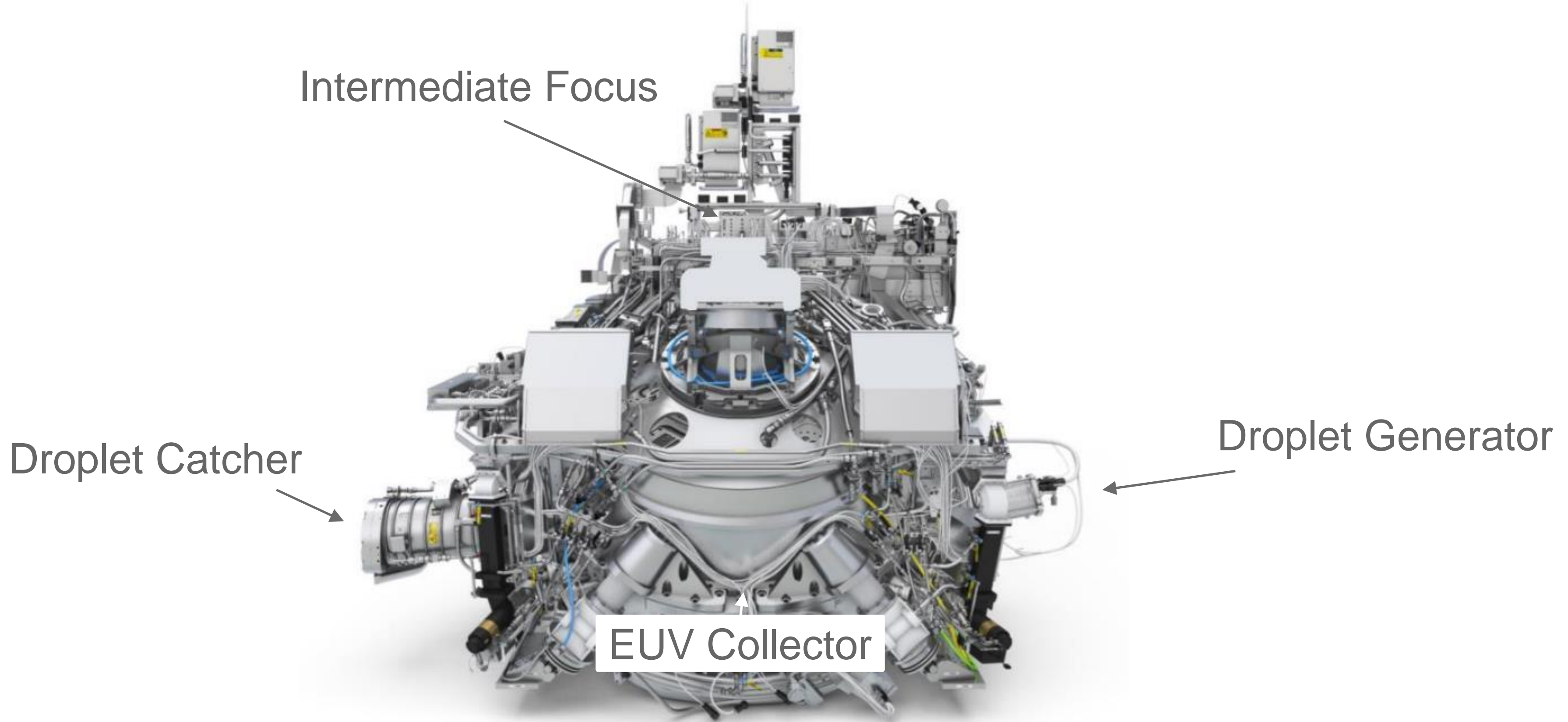
Hummingbird flap their wings
40-80 times in one second

Bees flap their wings
180 times per second

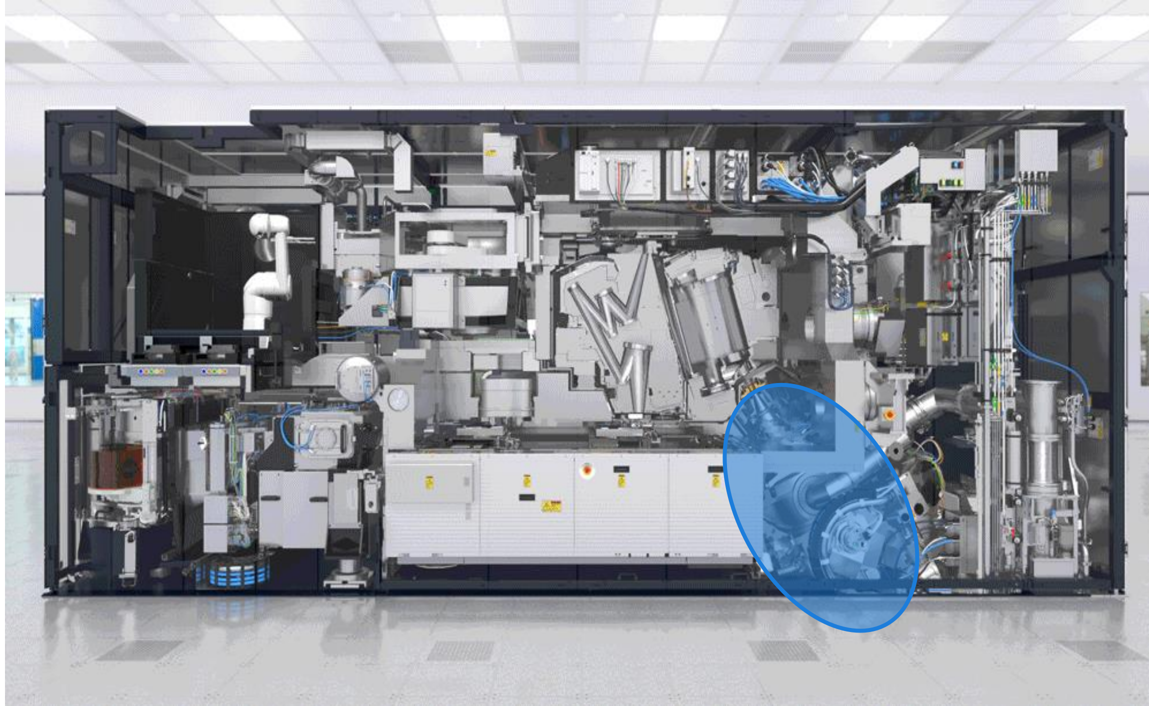
How about an internet second?: 54,907 Google searches, 125,406 YouTube video views and 2,501,018 emails sent (2016 data)

Main modules of the EUV Source

Populated vacuum vessel with tin droplet generator and collector



ASML EUV Lithography - expanding the possibility landscape by providing……………………..



Process simplification and improved device performance

15 to 50% cost reduction compared to multi-patterning schemes

3 to 6x cycle time reduction compared to critical multi-patterning layers

Best in class overlay performance and focus performance

EUV simplifies process complexity to enable our customers to drive cost effective pattern scaling beyond 7nm Logic and 16nm DRAM

ASML where it all happens

Veldhoven, the Netherlands

ASML Wilton Facility

ASML San Diego Facility

Zeiss Oberkochen Facility

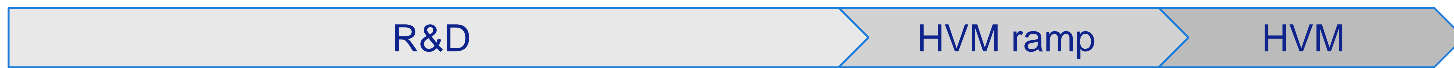
Our EUV journey so far…. > 10 years to develop EUV technology with our customers

2006	2010	2013	2017	2018-19
ASML ships first full field EUV research system	ASML ships first NA 0.25 development system NXE:3100	ASML ships first NA 0.33 development system NXE:3300B	ASML ships first NA 0.33 production system NXE:3400B	ASML NXE:3400B installed base >25 systems by end of 2018
28 nm Lines and spaces	19 nm Lines and spaces	13 nm Lines and spaces	7 nm and 5 nm node patterns	7 nm and 5 nm node patterns

Number of tools	**2**	**8**	**10**	**>25**
Availability	<10%	40%	70%	80% → 90%
Productivity	<1wph	<10wph	<50wph	125 → 155wph
Overlay	8nm	6nm	5nm	3nm →2.5nm

EUV technology now supporting processes of the future

Installed base of EUV systems ramping in preparation for HVM in 2019

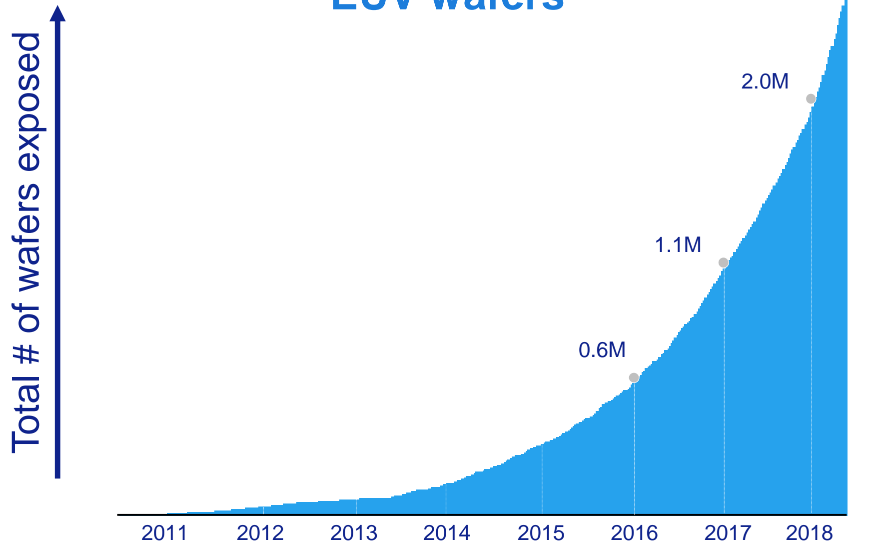


NXE:33x0 and NXE:3400

Installed Base
Planned
Shipments

Year	Shipments	Installed Base
'13	3	3
'14	4	7
'15	2	9
'16	3	12
'17	10	22
'18	18	40
'19	30 (planned)	

EUV ramp at our Logic customers has started with DRAM expected to begin in 2019



More than 3.2 Million wafers run since 2011…

… ~1 Million in the last 6 months

C.C.Wei, TSMC co-CEO @ 2Q18 earnings (July 2018)

"The silicon results from our N7+ today are very encouraging. Volume production will start Q2 next year, that is Q2 2019. We have made ready multiple EUV scanners to support not only the N7+ development, but also N5 development. Our silicon data have proved all the benefits we expect from process simplification with EUV. In addition, we have also started our N3 technology development."

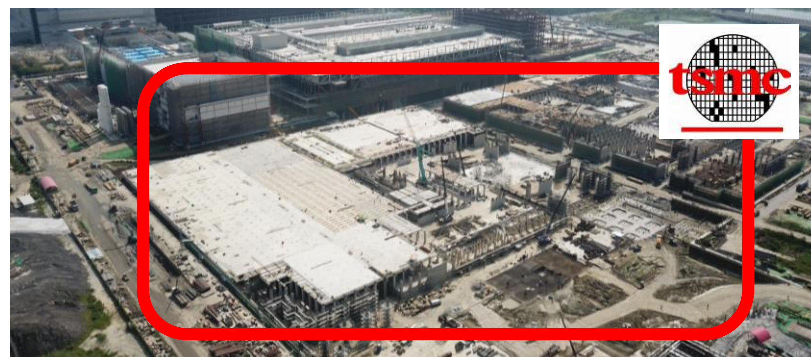
ES Jung, EVP Foundry Seoul October 18th, 2018

The initial EUV production has started in Samsung's S3 Fab in Hwaseong, Korea. By 2020, Samsung expects to secure additional capacity with a new EUV line for customers who need high-volume manufacturing for next-generation chip designs

Intel @ 1Q18 earnings (April 2018)

"…10 nm process…volume production is moving from the second half 2018 into 2019... we understand the yield issues. They're really tied to this being the last technology not having EUV, the amount of multi-patterning and the effect of that on defects…we have 4,5,6 layers of patterning to produce a feature.

Customers are building significant capacity for advanced processes using EUV systems



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Immersive devices will be the next computing wave

Source: Lisa Su, AMD, "Immersive era in consumer computing", IEDM, Dec. 2017

The revolution in automotive

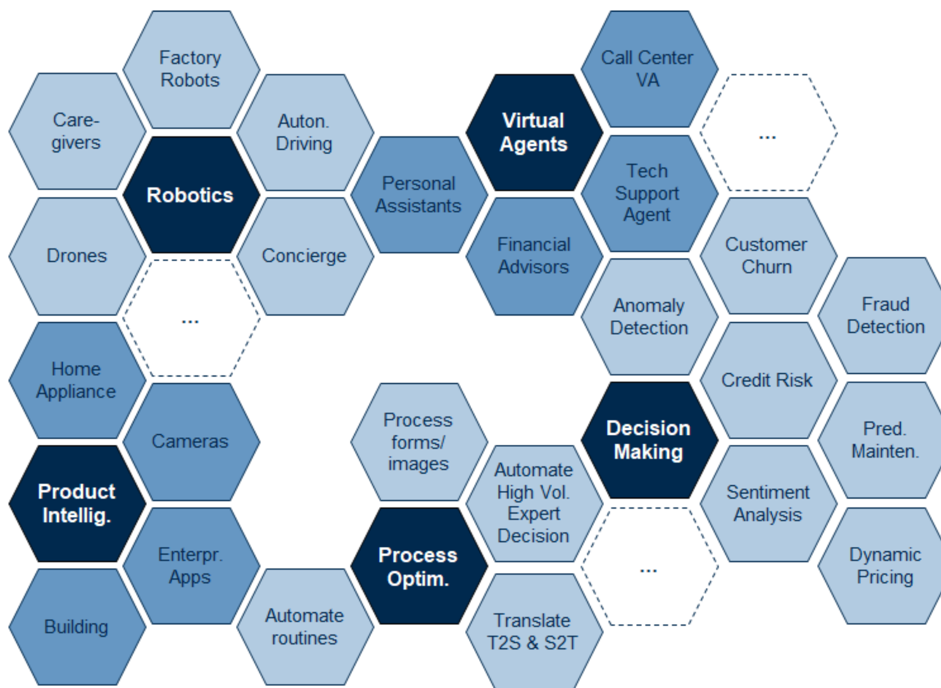
- Long-range radar
- LIDAR
- Camera
- Short-/medium-range radar
- Ultrasound/ultra-short-range radar

Environment mapping
Environment mapping
Surround view
Digital side mirror
Traffic sign recognition
Blind spot detection
Adaptive cruise control
Emergency braking
Pedestrian detection
Collision avoidance
Cross-traffic alert
Park assist
Park assist
Rear collision warning
Park assistance
Surround view
Rear view mirror
Environment mapping
Environment mapping
Lane departure warning
Blind spot detection
Surround view
Digital side mirror
Environment mapping
Environment mapping

Autonomous and connected cars drive double digit growth to 80 B$ by 2025

Source: NVIDIA Corporate Presentation 2018

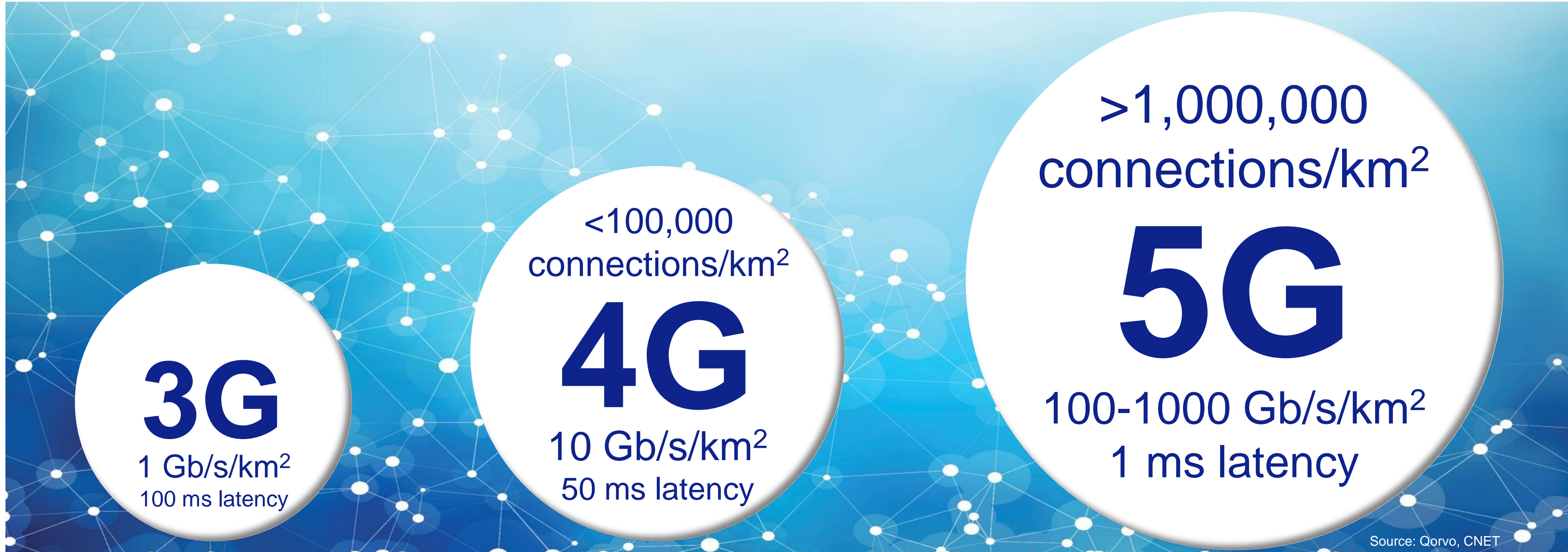
Artificial Intelligence impacting multiple applications



Artificial Intelligence (AI) as a major industry disruptor will represent a >15B$ new revenue opportunity in semiconductors by 2022

Source: Gartner

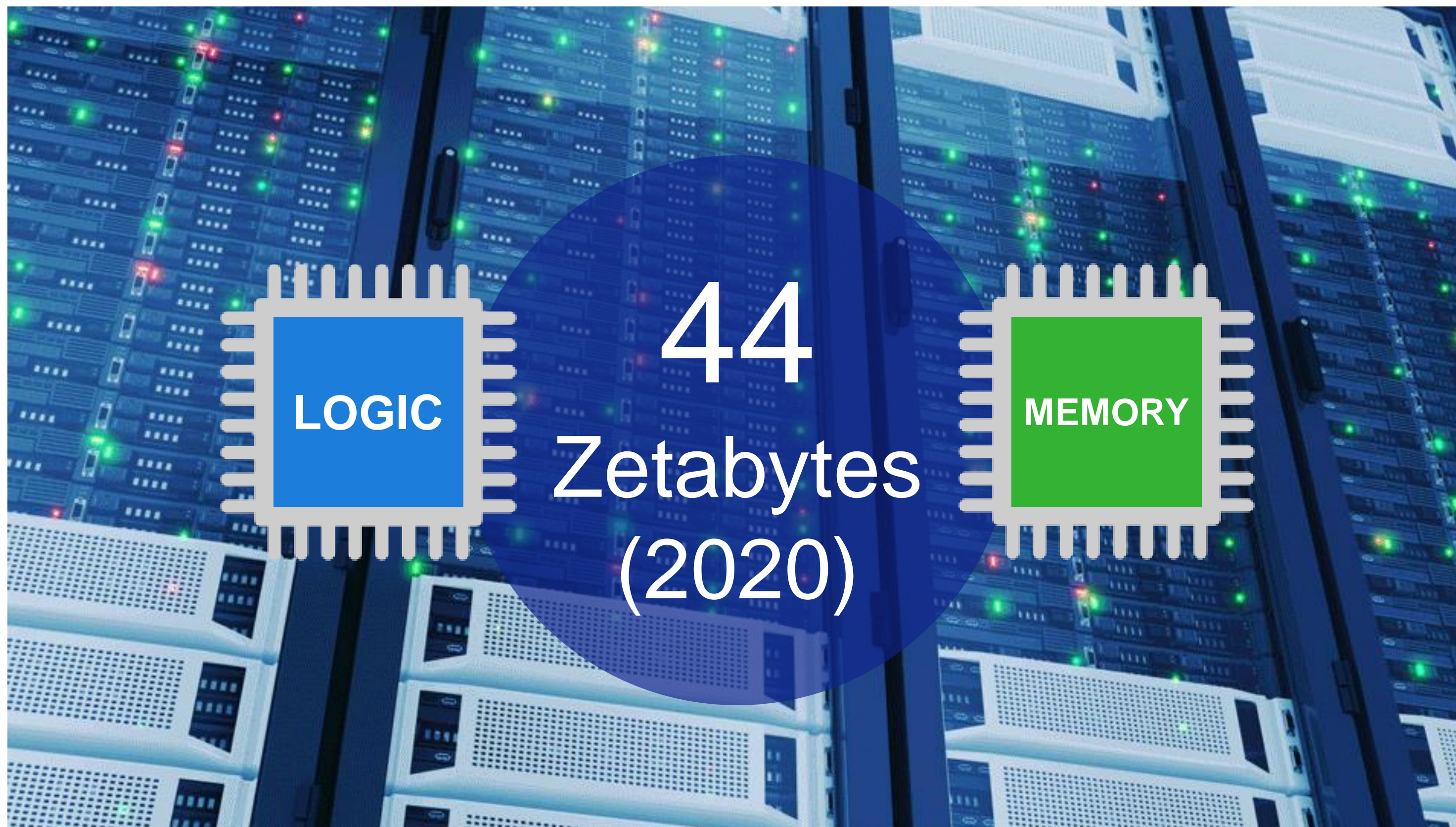
5G connectivity



5G connectivity speed and latency improvement drives applications with more volume and real-time use

Source: Several public sources

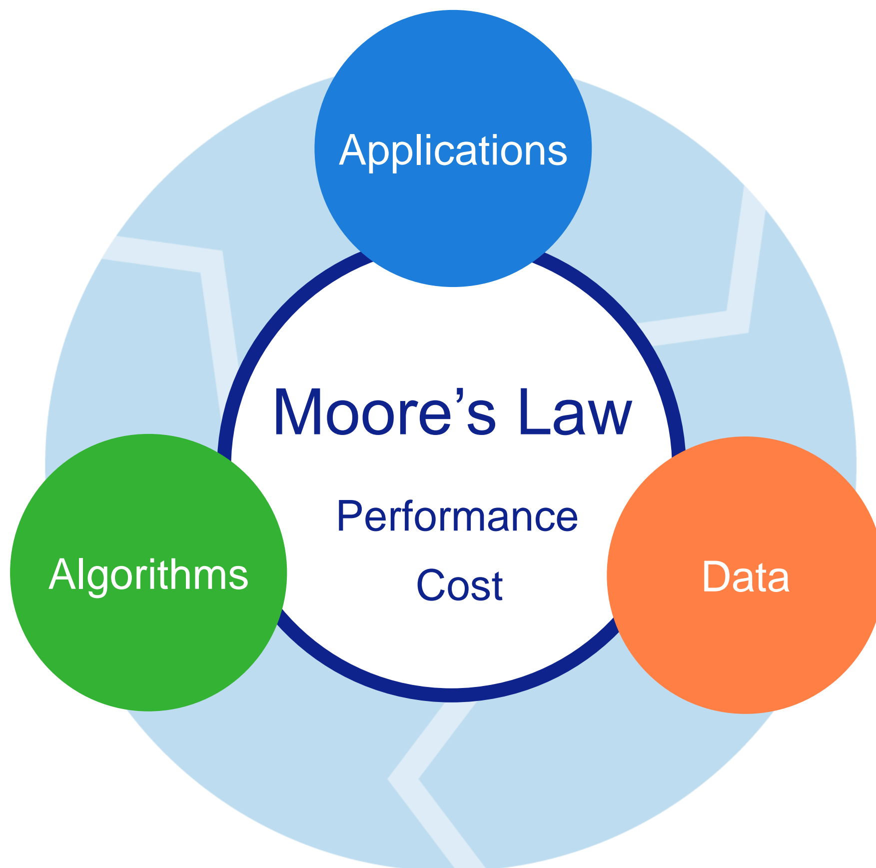
Advanced chips are needed to store and crunch data



Source: EMC Digital Universe report with Research & Analysis by IDC (2014)

Major trends in semiconductor-enabled computing

High demand is fueled by these major industry trends

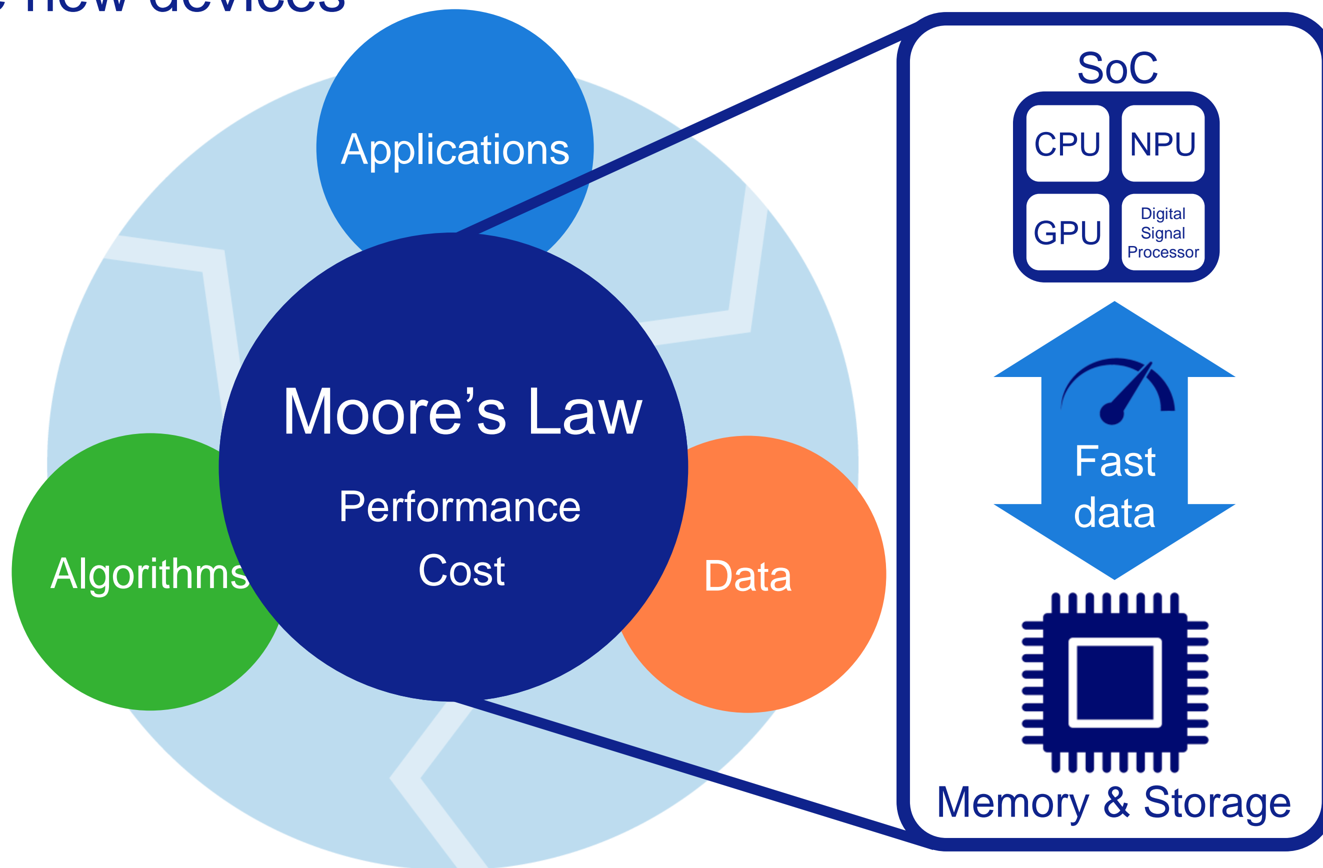


- Autonomous decisions
- Immersive resolution
- On-device Artificial Intelligence
- Virtual / augmented reality

- 5G connectivity
- Real-time latency
- Growing data volumes

- From big data to value
- Enhanced processing
- Deep learning

Major trends in semiconductor-enabled computing require new devices



Source: Sumit Sadana, Micron, Micron Investor Day, May 2018

ASML continues to enable Logic process evolution

APL0098	APL2298	A4	A5	A6	A7	A8	A9	A10	A11	A12
90nm	**65nm**	**45nm**		**32nm**	**28nm**	**20nm**	**14/16nm**	**16nm+**	**10nm**	**7nm**
XT:12X0 *Shrink* *Add functions*	*XT:14X0* *Shrink* *Add functions*	*XT:17X0I* *Shrink* *Add functions*	*Add functions*	*XT:19X0I* *Shrink* *Add functions*	*NXT:1950Ai* *Shrink* *Add functions*	*NXT:1960Bi* *Shrink* *Add functions*	*NXT:1970Ci* *Shrink* *Add functions*	*Add functions*	*NXT:1980Di* *Shrink* *Add functions*	*NXT:1980Di* *Shrink* *Add functions*
72mm²	**71.8mm²**	**53.3mm²**	**122.2mm²**	**97mm²**	**102mm²**	**87.4mm²**	**96-104mm²** (APL0898 Samsung 96mm²; APL1022 TSMC 104.5mm²)	**125mm²**	**89mm²**	**83mm²**
16 bit 1 Core 1 GPU 412 MHz	32 bit 1 Core 1 GPU 412 MHz	32 bit 1 Core 1 GPU 0.8 GHz	32 bit 2 Core 2 GPU 0.8 GHz	32 bit 2 Core 3 GPU 1.2 GHz	64 bit 2 Core 4 GPU 1.3 GHz	64 bit 2 Core 4 GPU 1.4 GHz	64 bit 2 Core 6 GPU 1.85 GHz L14&N16FF	64 bit 4 Core 6 GPU 2.37 GHz **N16FF+ InFO** wafer-level pckg	4.3B transistors 2 +4 Core CPU (4 + 1)GPU + NPU 2.4 GHz **N10FF**	6.9B transistors 2 +4 Core CPU (6)GPU +8 NPU 2.5 GHz **N7FF**

Source: ASML Market Research

And those processes continue to evolve and new devices are being designed and built now

ASML

TSMC with EUV process gearing up for AI, 5G boom

Monica Chen, Hsinchu; Jessie Shen, DIGITIMES

Friday 22 February 2019

Chipmakers are expected to showcase their new-generation chip solutions for AI and 5G applications at the upcoming Mobile World Congress (MWC) trade fair, with Taiwan Semiconductor Manufacturing Company (TSMC) being their major foundry partner thanks to the competitiveness of its EUV-based process technology, according to industry sources.

Huawei's HiSilicon, Qualcomm, Intel, MediaTek and Broadcom are all looking to line up their new products for handsets and mobile base stations, and other applications built on AI and 5G technologies at the 2019 MWC that kicks off on February 25.

Qualcomm is set to present its flagship Snapdragon 855 series mobile SoC that will power a number of new 5G smartphones slated for launch this year. Qualcomm will also showcase its Snapdragon X55 5G modem at the trade exhibition in Barcelona. Both chip solutions are reportedly manufactured using TSMC's 7nm FinFET process technology.

Huawei is expected to introduce its new Balong 5000 series smartphone equipped with 5G baseband developed by HiSilicon during the trade show next week, while MediaTek's lineup will include its Helio M70 and other 5G chip solutions, the sources said. HiSilicon and MediaTek both partner with TSMC to manufacture their advanced 7nm products, the sources said.

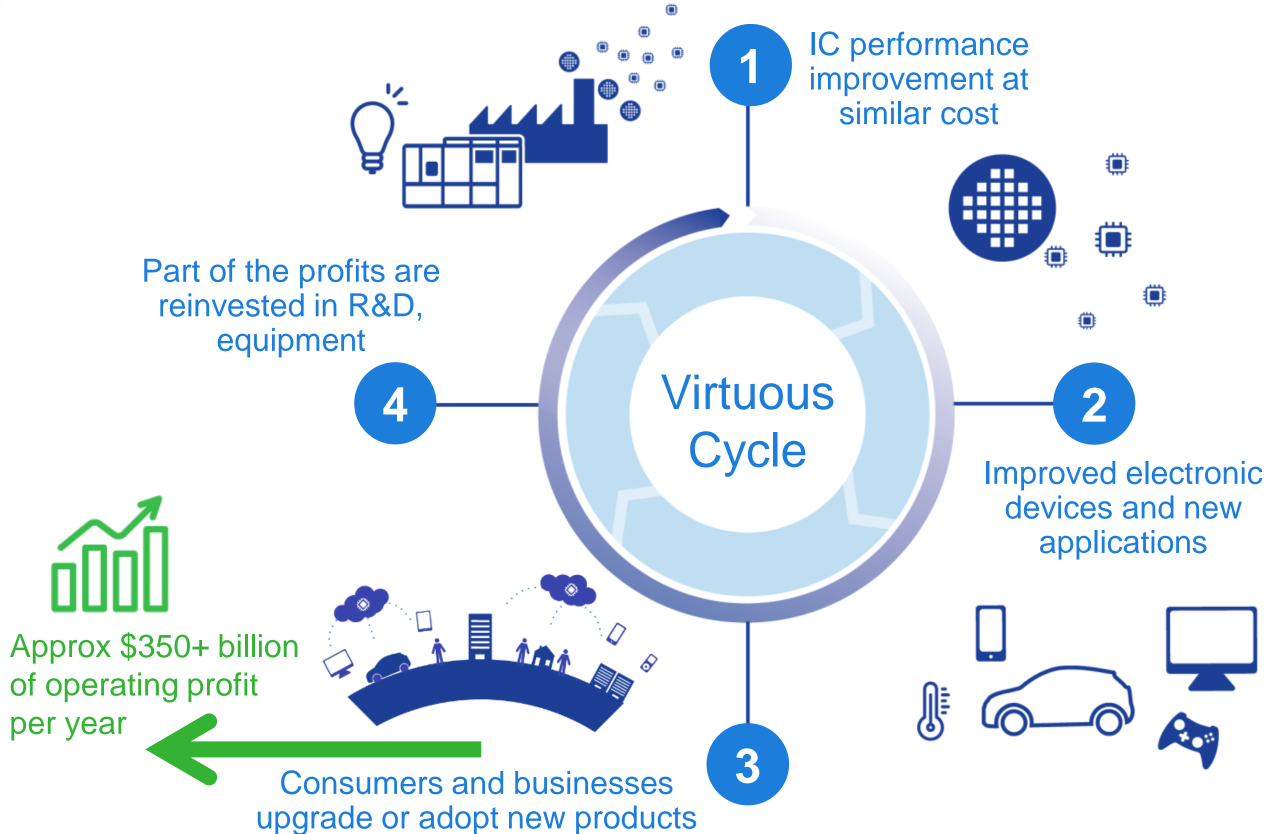
Meanwhile, 5G models presented by major smartphone vendors at the event will also highlight the currently available 7nm SoCs powering the devices, with TSMC being the major fabricator for those chip developers, the sources indicated.

In addition, TSMC has obtained 7nm chip orders for 5G related applications including HPC and IoT from AMD, Nvidia, Xilinx, NXP, OmniVision and TI, the sources added. TSMC is expected to secure the first 5nm chip orders from Apple for the 2020 iPhones, the sources continued.

TSMC expressed previously optimism about its performance in 2020 and 2021, when 5G and other emerging technologies mature. Despite its dim business and industry outlook this year, TSMC claimed it is making progress in the development of sub-7nm process technologies with plans to move a newer 5nm EUV process to volume production by 2020 well on track.

Considerable motivation to continue Scaling/Shrinking

Moore's Law is underpinning a business model



Takeaways

Approx $350 billion of annual profit is riding on the industry's ability to keep this cycle going

ASML operates in an industry value chain that has considerable means with strong incentives to compete and drive innovation

Top technology companies in our ecosystem (EBIT **CY2017**, B$)

Semi Equipment

Applied Materials	ASML	LAM Research	KLA-Tencor	TEL
4.3	2.8	2.6	1.4	2.2

Semi Manufacturers: Intel, TSMC 12.7, SK hynix 12.2, TI, Micron 8.7

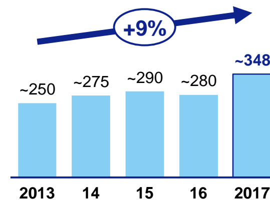
Semi Design: Intel 18.0, Samsung 47.6, NVIDIA 3.2, 6.1, Broadcom 2.4, Qualcomm 1.9

Hardware: Apple 64.3, Cisco 12.0, Foxconn Hon Hai 3.7, HP 3.6, Canon 3.0, 10.4

Software & Service: Google / Alphabet 26.1, Microsoft 30.8, Oracle 12.9, facebook 20.2, SAP 5.6, Alibaba 10.4, amazon 4.1, eBay 2.3, Cognizant, ADP, Baidu 1.6, Hitachi 5.6, IBM

Legend: ASML, Peers, Semi, Software

In our ecosystem, EBIT has grown at high single digit levels



Source: Bloomberg (GICS 45 classification)

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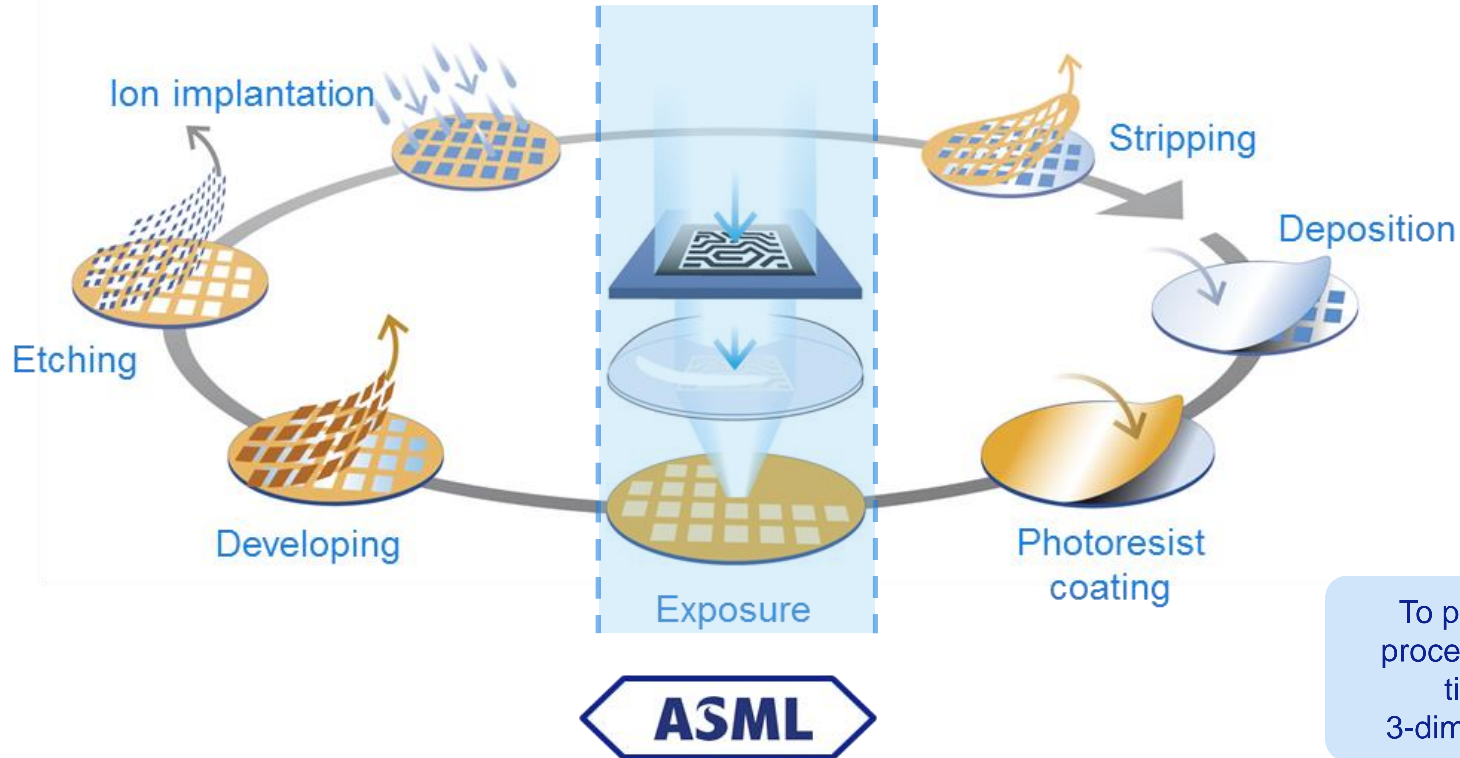
Lithography is and will remain at the heart of the semiconductor manufacturing process

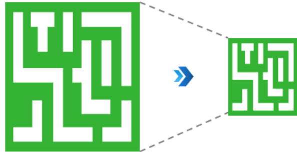


To produce a chip the process is repeated >50 times to build a 3-dimensional structure

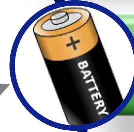
Power, Performance, Area, and Cost are critical requirements for scaling - Lithography is at the Heart

Industry role

ASML role

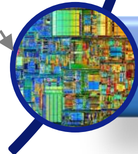


Increase performance — e.g. enable new computing architectures



Reduce power/energy — e.g. HVM integration of new materials

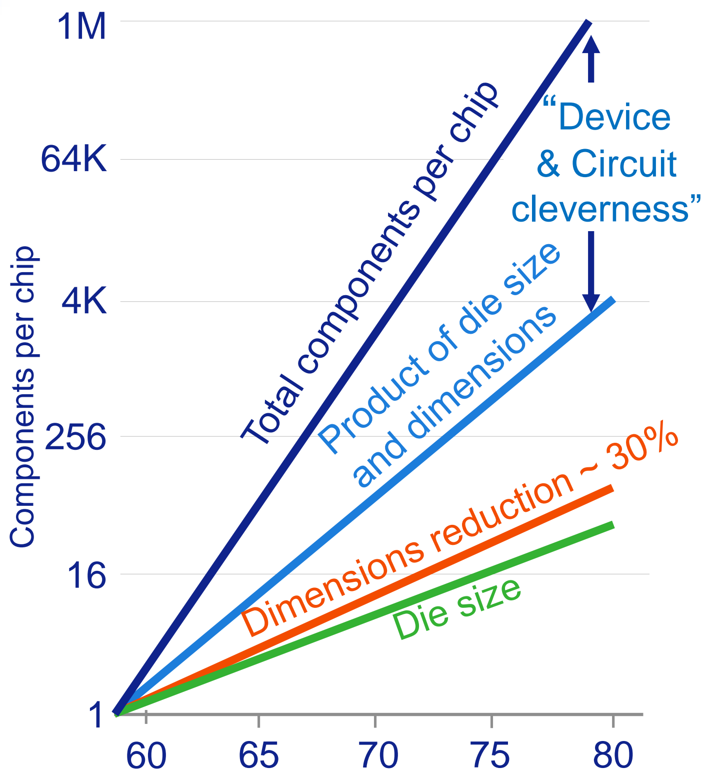
Reduce cost — e.g. improving yield with ASML Apps products

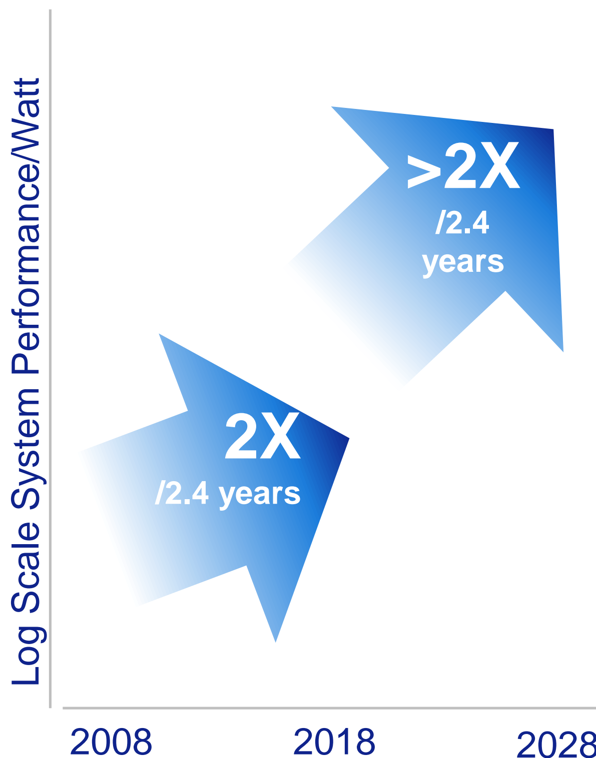


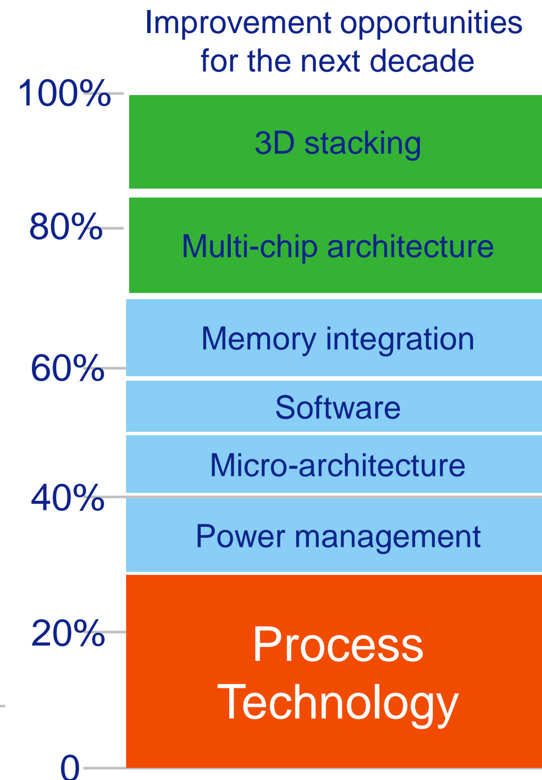
Reduce area — e.g. higher routing density by enabling litho, transistor stacking in HVM or 3D circuit structures.

Chipmakers accelerate performance for the next decade[1]

Process technology innovation accounts for 30%, grounded in Moore's prediction[2]

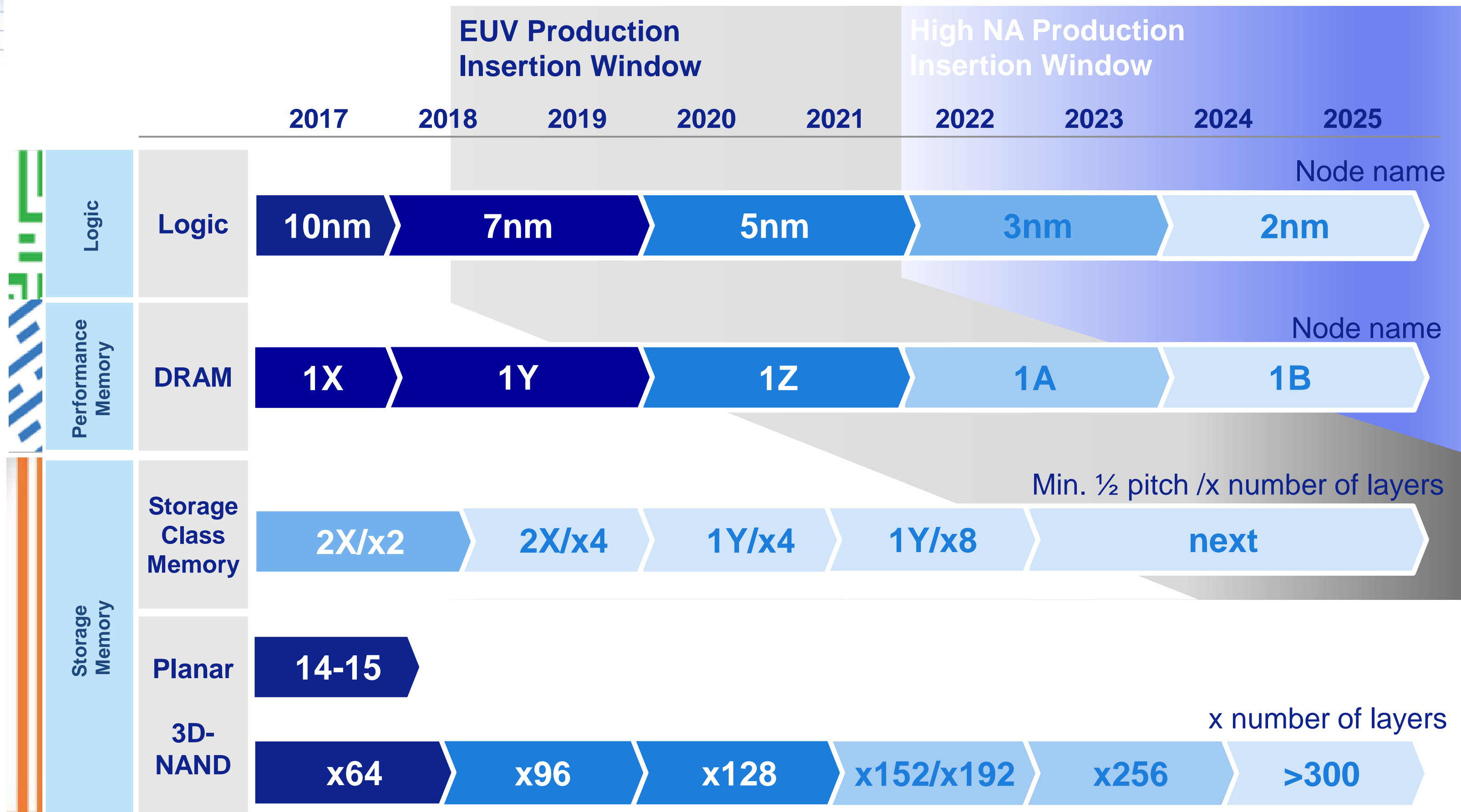






[1]Lisa Su, AMD, "Immersive era in consumer computing", IEDM, IEEE, dec 2017
[2]Gordon Moore, "Progress in digital integrated Electronics" International; Electronic Device Meeting,, IEEE, 1975, p p 11-13

Customers’ roadmaps show continued plans to shrink



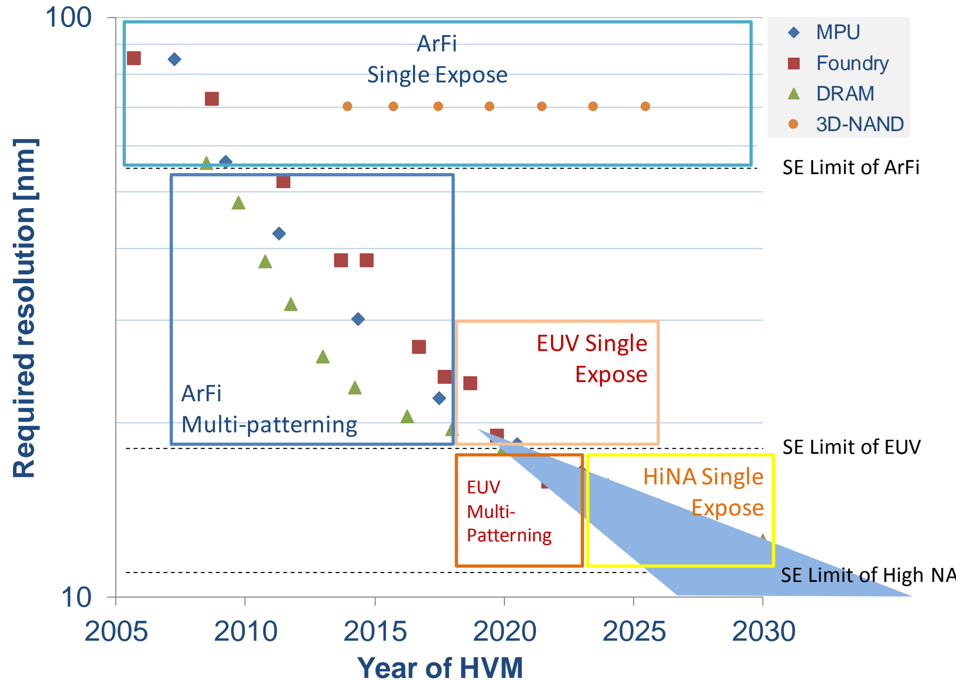
Today’s status
- Production[1]
- Development[1]
- Research[1]
- Roadmap[2]

Source: [1] Customers public statements, IC Knowledge LLC; [2] ASML extrapolations

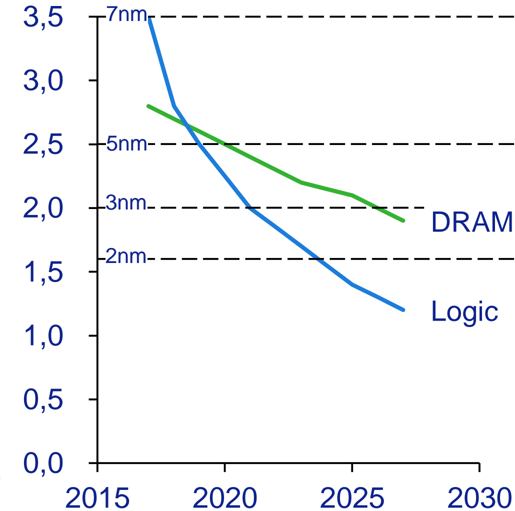
And ASML has a roadmap to match

Combined EUV, High NA, DUV and holistic solutions needed to support shrink in the next decade

Minimum resolution continues to shrink …



… and Logic takes over from DRAM in overlay scaling



Mix&match lithography	Applications
NXT:1980i NXE:3400B	YieldStar Software
NXT:2000i NXE:3400C	YieldStar Software
ArFi Next NXE:3400C	YieldStar Software
ArFi Next NXE Next	YieldStar Software

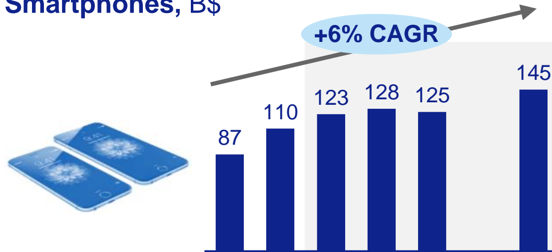
Customers request complementary product innovation

Source: ASML analysis

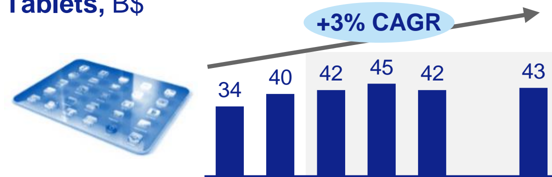
End market growth drives our opportunity

Mobile and PC maturing

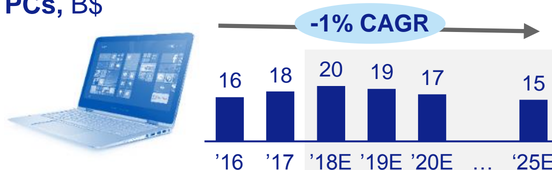
Smartphones, B$



Tablets, B$

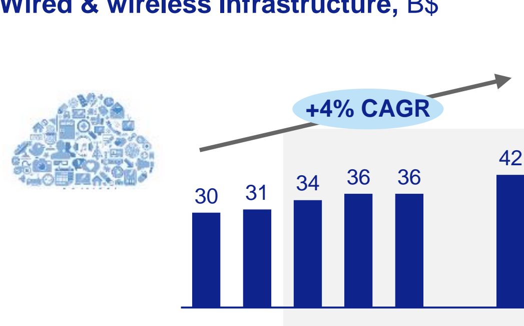


PCs, B$

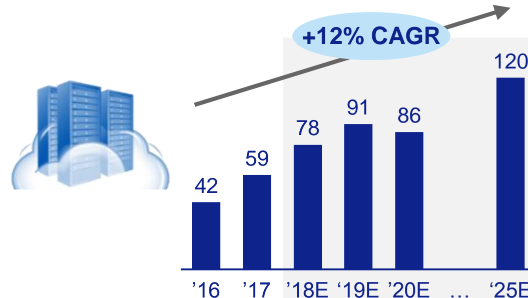


Continued growth in cloud applications

Wired & wireless Infrastructure, B$

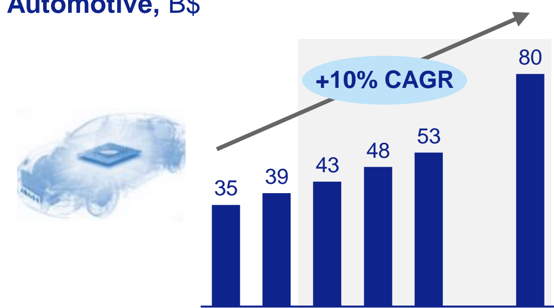


Servers, Datacenters & Storage, B$

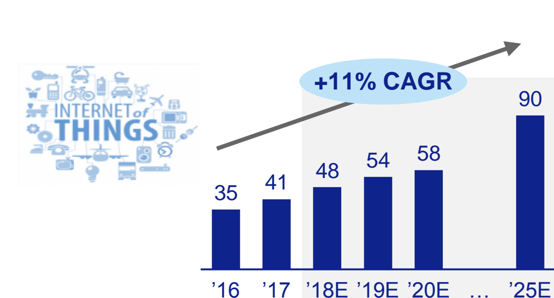


Emerging connected devices market

Automotive, B$

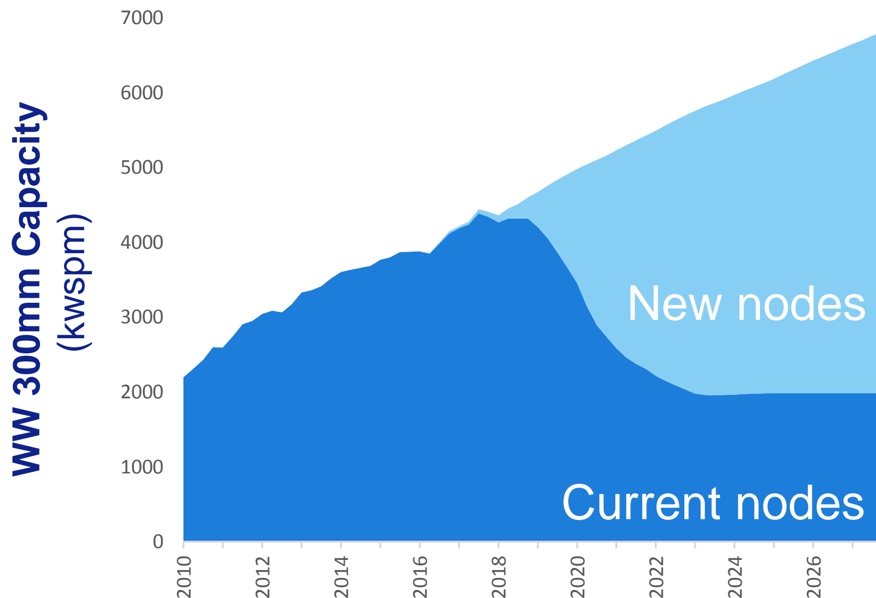


Industrial Electronics, B$



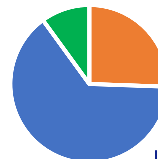
Source: Gartner through 2020, 2025 revenue extrapolated

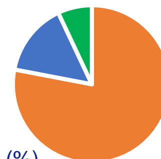
IC unit demand growth drives investments in wafer capacity
Most of which will be on leading edge nodes



- Growing wafer capacity drives increased litho demand
- New (leading edge) nodes with increased litho intensity further drives litho demand
- Conversion of existing nodes to new nodes also provide additional upgrade opportunity
- New process nodes will be two thirds of the 300mm wafer volume by 2025

Driving ASML system sales toward our high value, high market share products



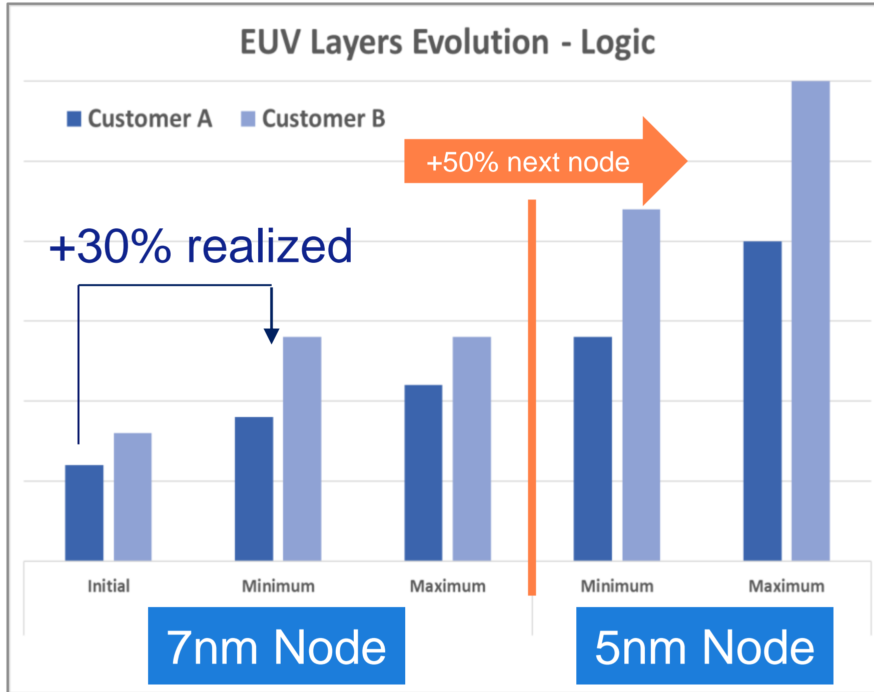


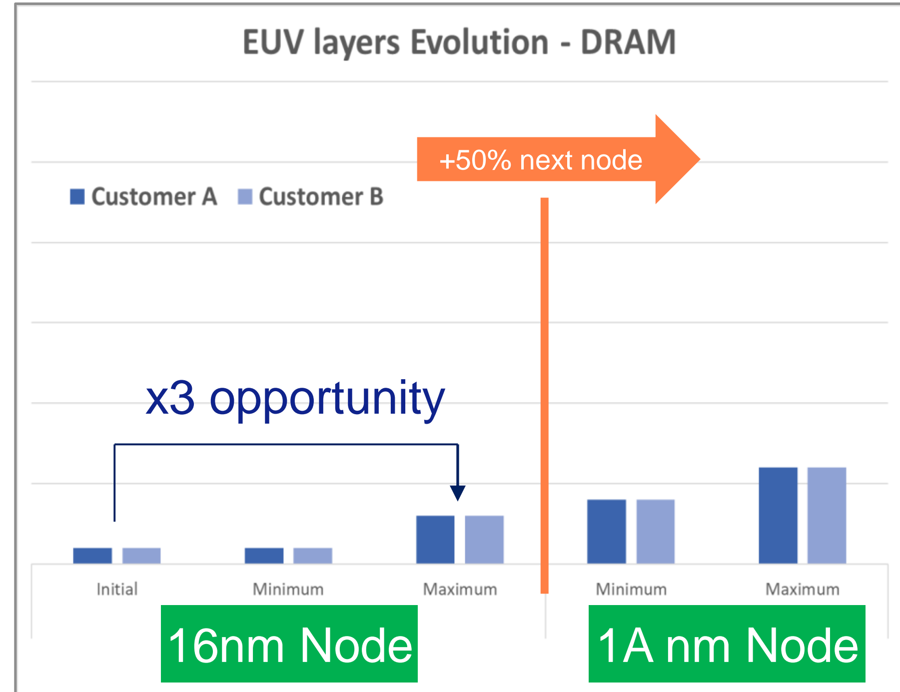
Litho Systems Revenue (%)

Source: ASML analysis

EUV continues to demonstrate its value

layer adoption increasing for Logic, expected EUV layer adoption DRAM





Logic adoption has increased by 30% for 7nm, 50% further layer adoption expected next node

Final DRAM layer adoption for first node still pending, significant increase expected at next node

EUV estimated demand per fab by market

Range of layers and corresponding systems per fab[1]

Market	Fab Capacity (kwspm[2])	EUV layers	EUV systems/fab
Logic (7nm – 5nm)	45	10 – 20	10 – 20
DRAM (16nm -1Anm)	100	1 - 6	2 - 10

Logic EUV capacity:

1 EUV layer requires 1 EUV system for every 45k wafer starts per month

DRAM EUV capacity:

1 EUV layer requires 1.5 to 2 EUV systems for every 100k wafer starts per month

[1] “Typical” process and system conditions in the 2018-2022 timeframe, not specific customer condition
[2] kwspm: x1000 wafer starts per month

EUV: two accelerated development programs in parallel

Supporting applications beyond the next decade

$$\text{Resolution} = k_1 \times \frac{\lambda}{NA}$$

EUV 0.33 NA

EUV 0.33 platform will be extended to provide state of the art overlay and node to node productivity improvements

2016 | 2017 | 2018 | 2019 | 2020 | 2021 | 2022 | 2023 | …2025

EUV
0.33 NA
13nm res

NXE:3350B
2.5nm | 125wph

NXE:3400B
2.0nm | 125wph

Overlay
1.5nm

TPut[1]
155

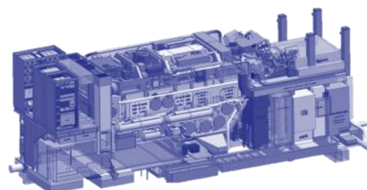
NXE:3400C
1.5nm | 170wph

NXE Next
<1.1nm | ≥ 185wph

0.55 NA
8nm res

High NA
1.1nm | 185wph

Product
Matched Machine Overlay|Throughput

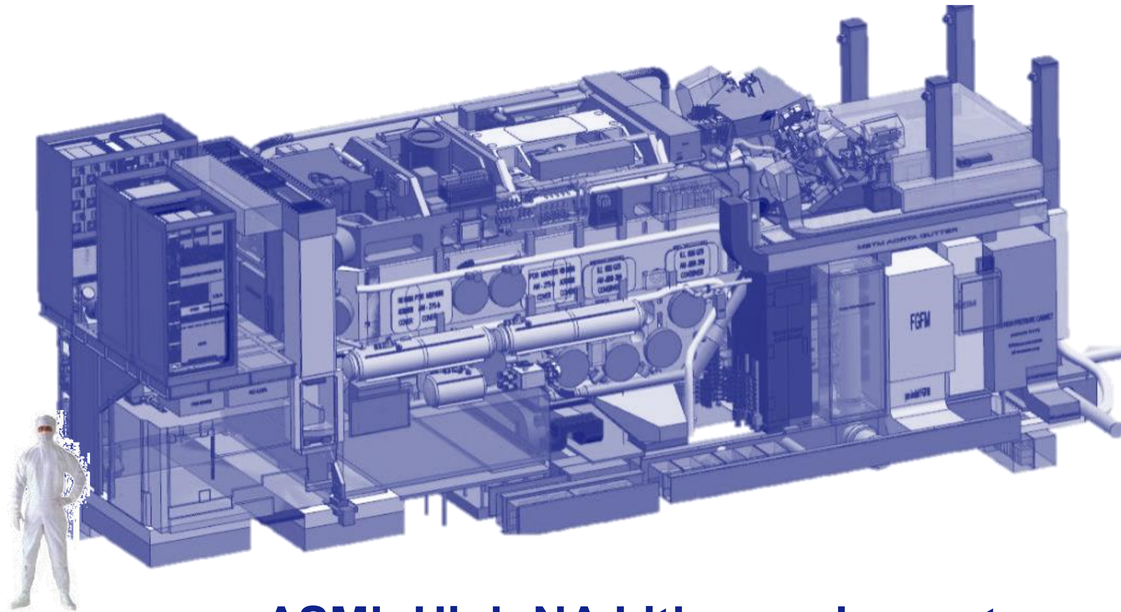


EUV 0.55 NA

High NA introduction at 3nm

[1] TPut: Throughput upgrade (wph)

In the same way 0.33NA enables 7nm Logic, 0.55NA EUV enables 3nm Logic



ASML High NA Lithography system

Process simplification and improved device performance

>> 50% cost reduction compared to multi-patterning schemes

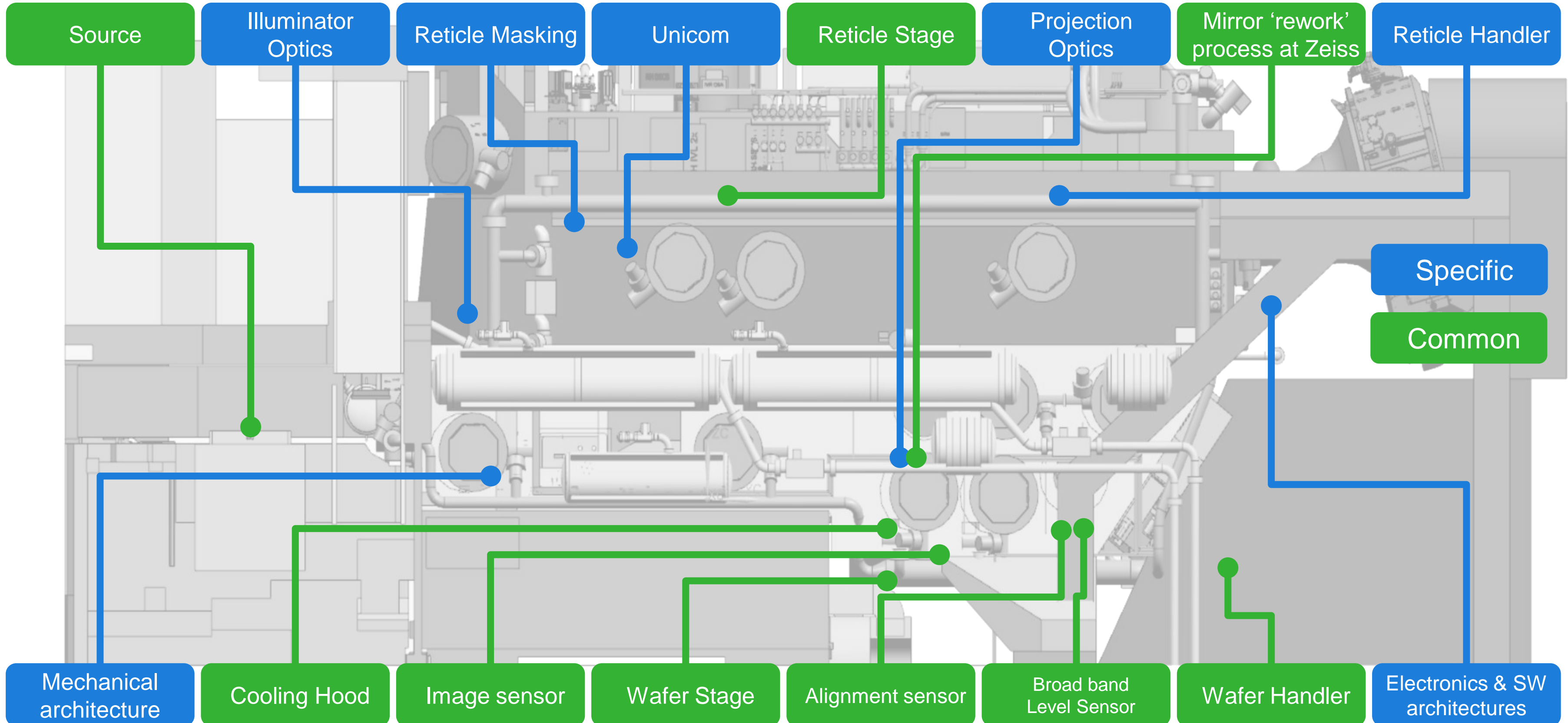
3 to 6x cycle time reduction compared to multi-patterning for critical layers

Best in class overlay performance and focus performance

We have received High NA commitment from 3 customers, for a total up to 12 systems

Reducing risk, lowering cost

Driving commonality between High NA and 0.33 NA

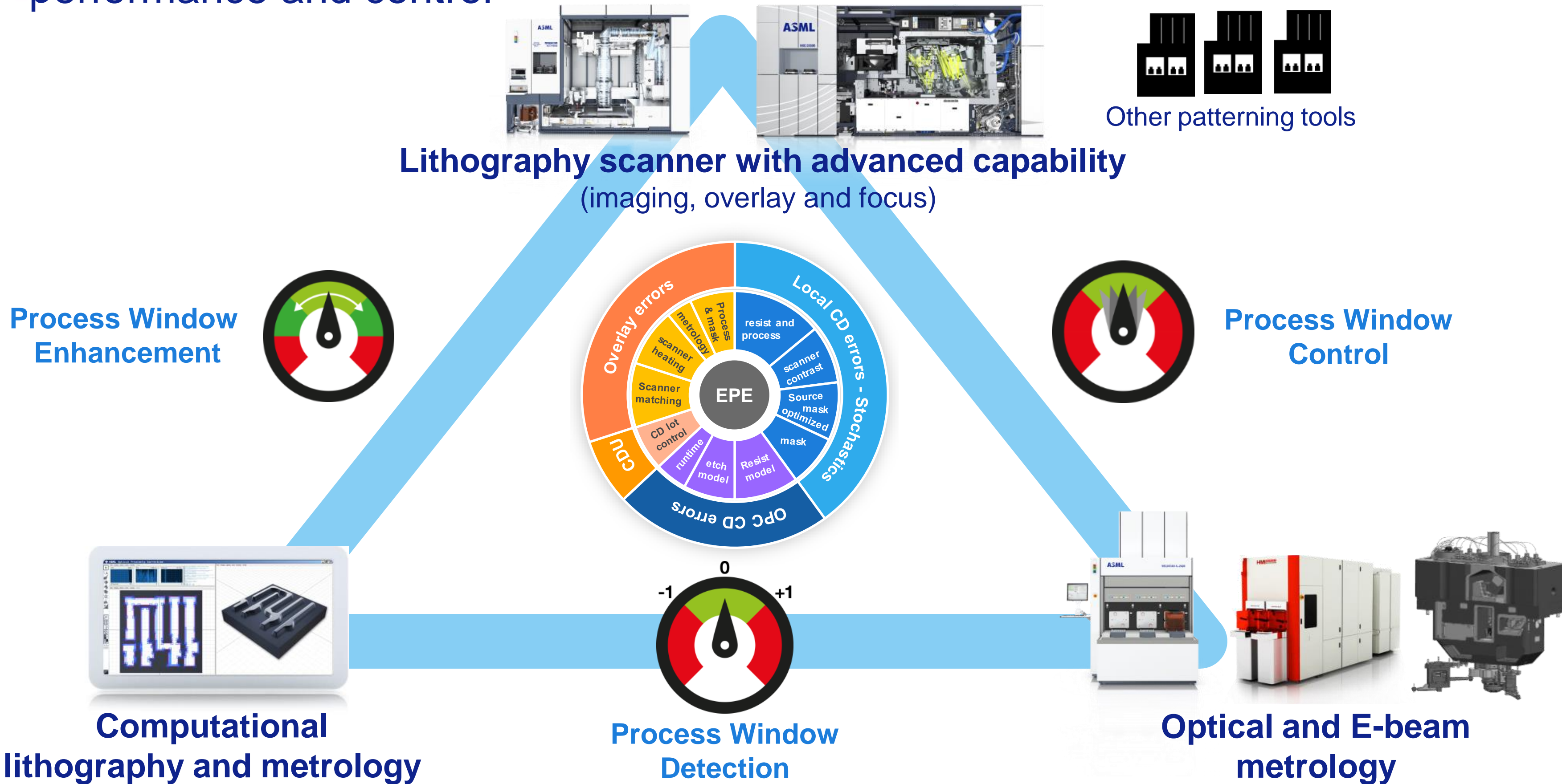


Solid progress to support optics development and manufacturing at ZEISS SMT

Optics metrology vessel installed in High NA cleanroom

Outer mirror handling robot

As Moore's Law continues, tolerance requirements get tighter ASML's Holistic Lithography roadmap focuses on patterning performance and control



ASML EUV Lithography - expanding the possibility landscape and providing a clear value creation opportunity

Semi End Markets

- Healthy semiconductor end market growth fueled by major innovation drivers such as 5G Connectivity, Artificial Intelligence, Autonomous Driving, and Big Data applications which demand miniaturization and extra functionality
- Translates into growth of world-wide fab capacity in all segments, especially at the leading edge nodes

Lithography Market

- Moore’s law continues to enable industry growth and lithography is a key enabler to cost effective shrink
- Strong growth opportunity in lithography beyond the next decade with a mix transition from DUV to EUV complimented by critical Holistic Litho process control solutions

Stakeholder Value

- We continue to execute our strategy and expand our product portfolio
- Further driving growth opportunities and delivering value to all of our stakeholders

ASML